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# Hazeltine ESPRIT™

## VIDEO DISPLAY TERMINAL MAINTENANCE MANUAL

HI-1100
December 1981

## SAFETY SUMMARY

### WARNING

Dangerous voltages (13,500 vdc, 600 vdc and 100 to 240 vac) are present in the Video Display Terminal. Some voltage may remain present in the monitor circuits after power is disconnected. Use caution when working on the interior of the terminal. Do not work alone.

Use caution when handling the cathode-ray tube (eg, wear safety goggles) to avoid risk of implosion. The internal phosphor coating is toxic; if the tube breaks and skin or eyes are exposed to phosphor, rinse with water immediately and consult a physician.

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APPENDIXES

## ILLUSTRATIONS



## TABLES

# SECTION I

# INTRODUCTION AND GENERAL DESCRIPTION

## 1.1 INTRODUCTION

This manual provides maintenance instructions for the Hazeltine Esprit Video Display Terminal. The contents of this manual may not reflect the latest changes in the product. Confirmation and any required clarification of this information should be obtained from:

Hazeltine Corporation
CTE Technical Support Dept.
Greenlawn, NY 11740
Telephone (516) 549-4624

Additional information and operating instructions are provided in the Reference Manual (HI-1094).

## 1.2 GENERAL DESCRIPTION

The terminal is a self-contained unit with keyboard, logic, monitor and power supply in a single chassis. Technical characteristics are summarized in Table 1-1.

### 1.2.1 Interface Controls

Eighteen DIP switches (figure 1-1) at the rear of the terminal select the terminal interface characteristics as follows:

Bank 1 switches 1, 2 and 3 cause foreground data to be displayed in high intensity, reverse video, and underlined, respectively and any combination may be used. They are effective only in the Hazeltine emulation mode (all data is low intensity in other modes).

Switches 4 and 5 enable or disable current loop for received and transmitted data respectively.

Switch 6 is set to select ∿ or ESCape as the lead-in character for Hazeltine mode only. If ESC is selected, ∿ (tilde) is a displayable character; if ∿ is selected it will not display.

Switches 7 and 8 select one of three emulation modes: Hazeltine, Lear-Siegler ADM-3A[1], or ADDS Regent 25[2].

The character selected by switches 9 and 10 (Carriage Return, End of Text, End of Transmission, or Null) will be transmitted (followed by a null) after any batch transmission, and after any terminal reply to a remote command (Send Cursor Address or Send Character at Cursor). In half duplex operation, a null will be transmitted after the selected character and Request to Send will drop.

---

1. Trademark of Lear-Siegler Corp.
2. Trademark of Applied Digital Data Systems

Table 1-1. **Technical Characteristics** (Sheet 1 of 2)

| | |
|---|---|
| **DISPLAY FORMAT** | |
| Screen | 12 inch (305 mm) diagonal, P146 (green) phosphor, raster scan |
| Capacity | 80 characters/line x 24 lines (1920 characters) |
| Character Format | 7 x 9 dot matrix in 9 x 12 window, dual intensity. Character shows through cursor in reverse video when superimposed. |
| Cursor | Block or underline; steady, slow or fast blink (keyboard selectable) |
| Character Set | 95 displayable ASCII, all 128 ASCII characters can be displayed in monitor mode |
| Refresh Rate | 60 Hz or 50 Hz, no interlace |
| TV Line Standard | 307 lines/frame (60 Hz) or 369 lines/frame (50 Hz) 288 lines displayed |
| Memory | 2048 x 8 Random Access Memory |
| **INTERFACE** | |
| Input/Output | EIA Standard RS 232 or 20 mA current loop at 110, 300, 600, 1200, 2400, 3600, 4800 or 9600 Baud, switch selectable |
| Auxiliary I/O | RS 232 with keyboard or remote output enable/ disable |
| Parity | Odd, Even, One (Mark), or Zero (Space), switch selectable |
| Character | 10 or 11 bit (start bit, 7 bit ASCII, parity, minimum of 2 stop bits at 110 baud, 1 at all other rates) |
| Modes | Half or full duplex, interactive or batch |
| **PHYSICAL/ENVIRONMENTAL DATA** | |
| Dimensions | 13.6" (340mm) H, 17.5" (440mm) W, 22" (550mm) D 30 lbs (13.5 kg) |
| Power | 115 V/60 Hz or 230 V/50 Hz, 40 watts (136 btu/hr) |

Table 1-1. **Technical Characteristics** (Sheet 2 of 2)

| | |
|---|---|
| Environment | Operating: 10° to 40°C (50° to 104°F), humidity 5 to 95% non-condensing. Storage: 0° to 65°C (32° to 150°F) |

## ADDITIONAL FEATURES

| | |
|---|---|
| Keyboard | Typamatic keyboard with 14 key numeric pad. Key click selected or cancelled from keyboard. |
| Self Test | Automatic self test at turn-on with specific fault indications plus keyboard entered memory test. |

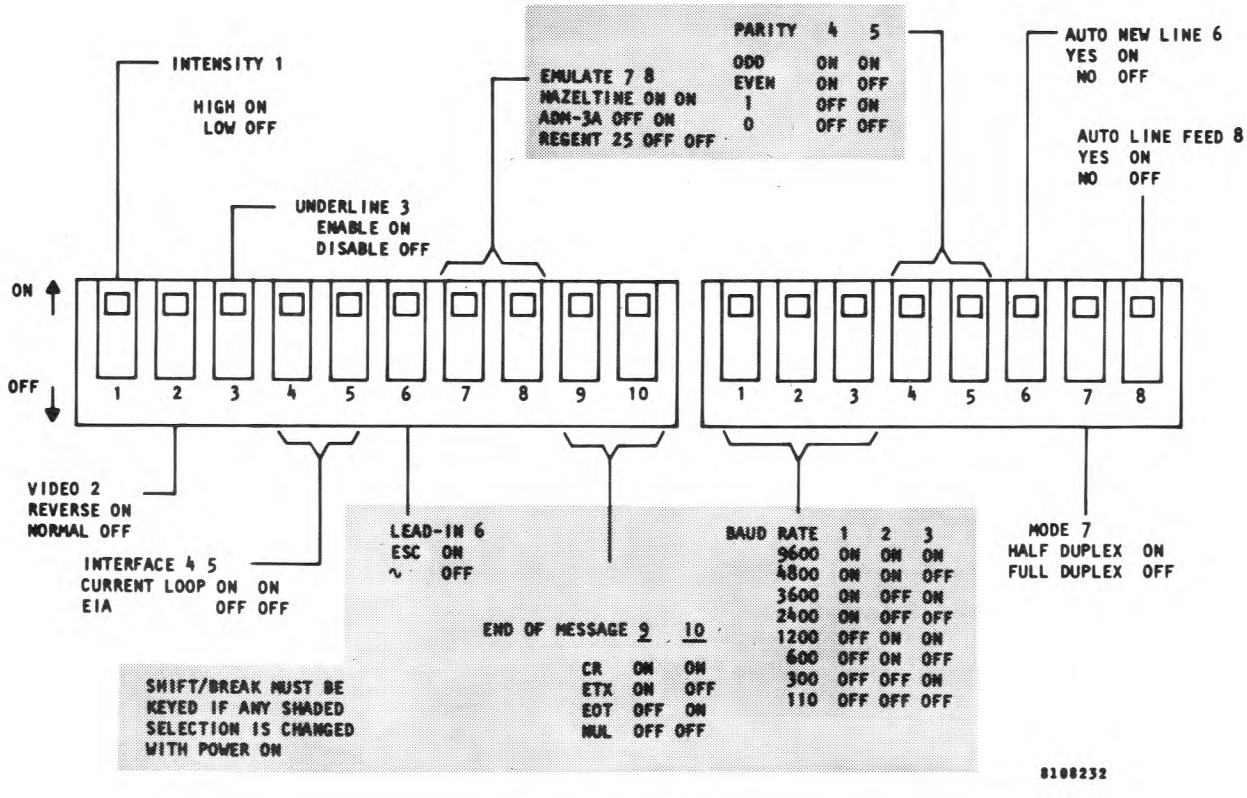



Figure 1-1. **DIP Switches at Rear of Terminal**

Bank 2 switches 1, 2 and 3 select one of eight Baud rates.

Switches 4 and 5 select one of four parity options for both transmitted and received data. If odd or even is selected the terminal will check received data for parity and display ? if an error is detected. No parity check is made if 1 or 0 is selected.

If switch 6 is on the cursor will automatically wrap from the last column of the display to the first column of the next line (Auto New Line). If the switch is off, when the cursor reaches the 80th column it will remain there, overwriting old data with new, until a cursor movement command is received.

Switch 7 selects half or full duplex operation.

If switch 8 is on the terminal will perform a Carriage Return **and** Line Feed for each CR received or entered and will ignore Line Feeds. If the switch is off, each CR will cause the cursor to move to the start of the **present** row and each LF will cause it to move down one row.

### 1.2.2 Modes of Operation

The terminal has three modes of operation which apply to all three emulations and two which apply only to Hazeltine emulation. The three are:

**Normal (Interactive)** in which keyboard data is transmitted when entered, and in half duplex, is displayed if character data and performed if a command. In full duplex only received or echoed data is displayed or acted upon. Received control characters are ignored except for valid remote commands.

In normal mode the emulation selected by DIP switch determines the characteristics of the terminal. When Hazeltine emulation is selected it is basically an emulation of Hazeltine 1500 operation; keyboard entered data is normally foreground and displayed as selected by DIP switch Bank 1 switches 1, 2 and 3 (paragraph 1.2.1). When ADM-3A or Regent 25 emulation is selected, all data is displayed as low intensity and the remote command set for the selected terminal applies.

**Monitor (Transparent)** in which all characters, including control codes, are displayed. Control characters display as a two character mnemonic in a single character window (Appendix A). The only function which is executed is a Carriage Return, which is both displayed and performed. Note that since Line Feeds are not performed, Auto Line Feed must be selected by DIP switch to use this mode. It may also be necessary to select Auto New Line (wraparound) to prevent data from overrunning the line length.

**Local** mode in which received data is ignored and keyboard data is displayed but not transmitted. Local may be Normal (commands executed and control characters ignored) or Monitor (control characters displayed as described above).

The two modes applicable to Hazeltine only are:

**Block/Page** in which keyboard data is stored, but not transmitted until the ENTER key is depressed, at which time all foreground data on the displayed page is transmitted. This is an emulation of the Hazeltine 1510/1520 "Format/Page Transmit" mode.

**Line** is a special case of block mode in which keyboard data is stored and all foreground data on the line the cursor is on is transmitted when either RETURN or ENTER is depressed. This is an emulation of the Hazeltine 1510/1520 "Format/Line Transmit" mode.

As shown in figure 1-2, there are limitations on changing operating modes. Local may be entered from Normal or Monitor modes and will retain the characteristic (display control codes or not) but there is no Local/Block mode. Block/Page mode can only be entered when Hazeltine emulation is selected and Line mode can only be entered if the terminal is already in Block/Page mode. The remote "Reset Block Mode" command or "BLOCK OFF" keyboard entry will return the terminal to Normal (Interactive) mode from either Block/Page or Line mode.

### 1.2.3 Keyboard Commands

Several features of the terminal are selected or disabled by keyboard entries as follows:

The BLOCK ON/OFF key, when depressed with the SHIFT key, places the terminal in Block/Page mode (functions only in Hazeltine emulation). Depressing the key without SHIFT returns the terminal to Normal mode from either Block/Page or Line modes. The "BLOCK" LED will be lit whenever the terminal is in either batch mode.

The AUX ON/OFF key, when depressed with SHIFT, enables data output at the Auxiliary I/O port (input is always enabled). Depressing the key without SHIFT disables auxiliary output. The "AUX" LED will be lit whenever auxiliary output is enabled.

The LOCAL key, when depressed with SHIFT, will alternately enable and disable Local mode (does not function in Block modes). The "BLOCK" LED will blink while the terminal is in Local mode.

The BREAK key, depressed with SHIFT, causes the terminal to transmit a 250 ms break signal (constant space) and also causes it to reread the DIP switches and reset any functions which have changed.

Each of the numeral keys on the main qwerty pad (not the numeric pad), when depressed with CTRL, performs a function as follows:

| | |
|---|---|
| c1 | Enter Monitor mode (does not function in Block modes) |
| c2 | Exit Monitor mode |
| c3 | Enter or Exit Line mode (toggle) (must be in Block mode) |
| c4 | Enable or Disable key click (toggle) |
| c5 | Select static cursor |
| c6 | Select slow blinking cursor |
| c7 | Select fast blinking cursor |
| c8 | Select block cursor |

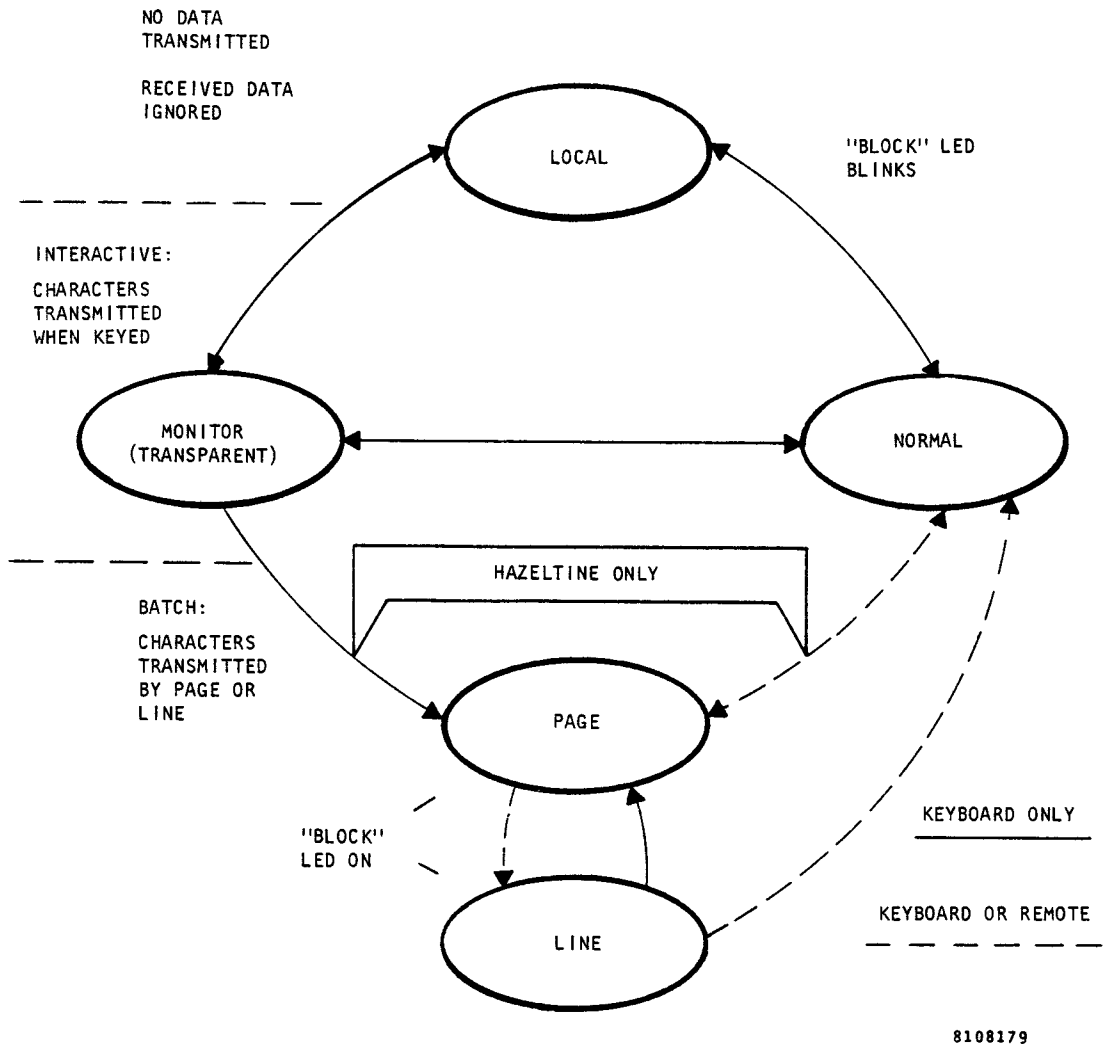



Figure 1-2. **Terminal Operating Modes**

$^{c}9$ Select underline cursor

$^{c}0$ Display memory test (does not function in Block modes)

The display memory test will alternately fill display memory with $55_H$ (background U's) and $AA_H$ (foreground *'s). These codes are complements and result in storing both a 1 and a 0 in every bit location.

**NOTE**

A subscript H is used to indicate hexadecimal notation throughout this manual. A superscript c or s indicates depression of a key with the CRTL and/or SHIFT key down.

### 1.2.4 Physical Description

The terminal contains four circuit boards in a single chassis (figure 1-3). The main logic board contains the microprocessor which controls all terminal functions; the I/O circuits which are responsible for external serial communication, reading the DIP switches, generating the alarm and key click tones, and controlling keyboard scanning; and the TV circuits (CRT controller, display memory and character generator) which control generation and refresh of the CRT display. The keyboard is on a separate circuit board. Each key is at a unique XY junction of a 10 x 8 scanning matrix. Under direction of the microprocessor, via the I/O logic, the scanner is made to excite one X line at a time. A signal will be returned (Y) to the microprocessor if any key on that line is depressed. When a key depression is detected the microprocessor consults a look-up table in ROM to determine the character code corresponding to that key. The TV logic on the main logic board generates the video signal, horizontal sync and vertical sync signals to the TV monitor. The monitor printed circuit board contains the video amplifier, and horizontal and vertical oscillators and the flyback transformer. It provides the video signal to the CRT cathode, the horizontal and vertical deflection signals to the yoke, and a 13.5 Kv anode voltage to the CRT.

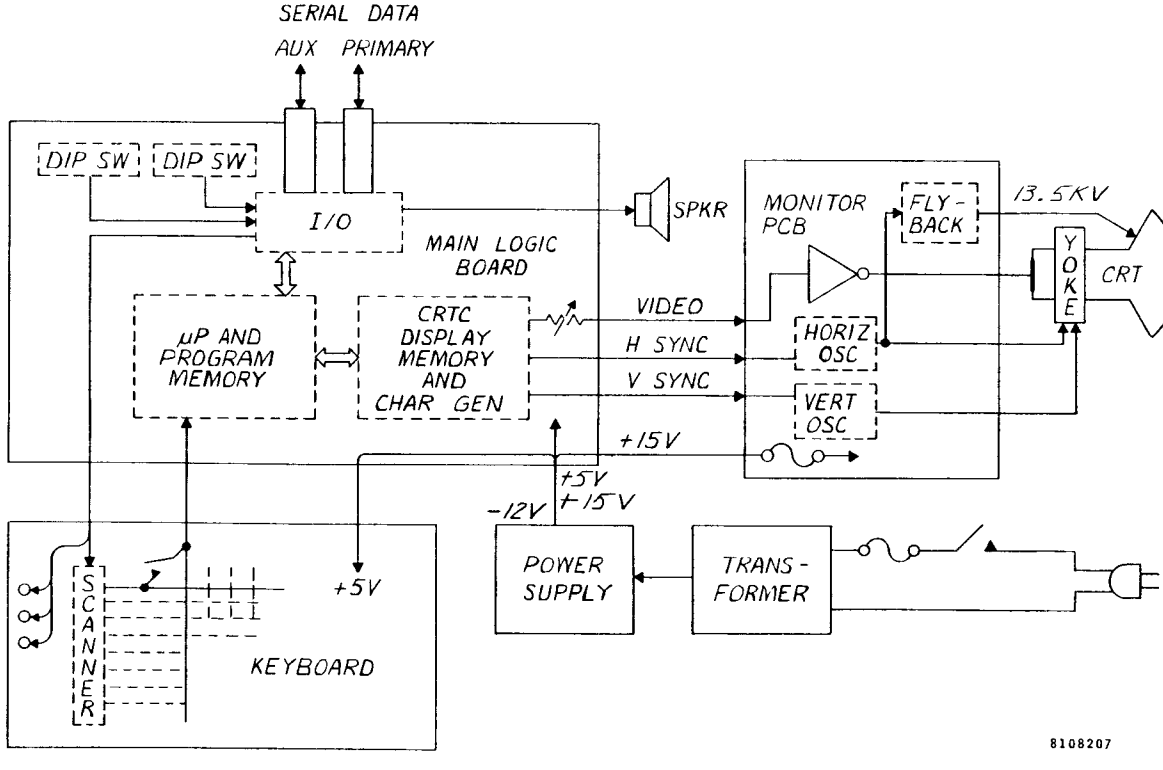



Figure 1-3. **Terminal Simplified Block Diagram**

Power for the circuit boards is provided by a separate power supply board which rectifies voltages from the power transformer to provide +5 Vdc, +15 Vdc and -12 Vdc for the other boards. Plus 12 Vdc for the EIA output drivers is derived from the +15 Vdc on the main logic board.

### 1.2.5 **Display Generation**

The CRT display is generated by the raster scan method from character fonts stored in a character generator ROM. Each character occupies a 9 dot wide by 12 dot deep window. An 8 x 12 dot font for each of 128 characters is stored in a ROM (actually 8 x 16, but the four highest bytes are never accessed). The top line and first column are always 0's (no dot). The CRTC reads the ASCII code for the next display location from display memory and uses it as the most significant 7 address bits to select the corresponding character font in the ROM (figure 1-4). The CRTC also generates a raster line count (0 to 11 for each character row). The raster count is the 4 least significant bits of the ROM address and selects the appropriate line to be displayed. The 8 bit byte addressed is then clocked out serially to become the video signal and generate the display. The ninth dot of the character window is always zero and is a ground on the serial input.

The CRTC is responsible for synchronizing the horizontal TV scan and vertical retrace with the character video, and also generates the cursor when the character window being refreshed corresponds to the cursor address loaded into its register by the microprocessor.

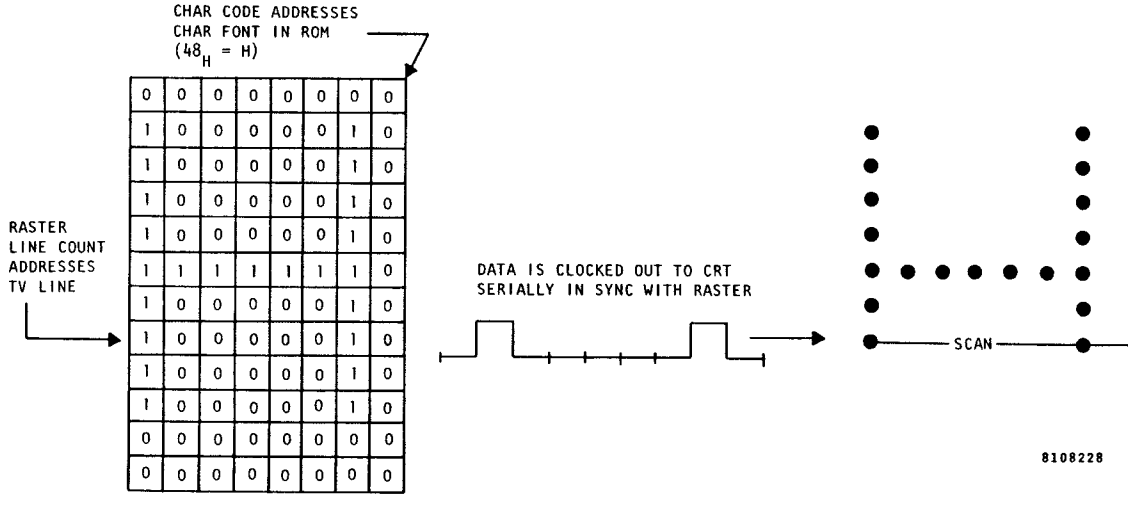



Figure 1-4. **Character Video Generation**

# SECTION II

# THEORY OF OPERATION

## 2.1 MAIN LOGIC BOARD

### 2.1.1 Introduction

The main logic board design is based on five large scale integration (LSI) circuits (figure 2-1); the microprocessor group, consisting of the Rockwell R6502 processor (U8), program ROM (U19), and the R6531 RAM, Counter, I/O chip (U20); the MC6845 CRT Controller (CRTC); and the MC6850 Asynchronous Communications Interface Adapter (ACIA) (U40). The microprocessor group controls the terminal by executing the instructions stored in the ROM. The CRTC synchronizes and refreshes the display based on parameters down loaded in its registers by the processor during the turn-on/initialization sequence. Both the processor and the CRTC share the 2K x 8 display memory. The ACIA converts data to be transmitted from parallel to serial and transmits it with the selected parity and stop bits at the desired baud rate, and converts received serial data to parallel and signals the microprocessor, by a data ready interrupt, when a character has been received.

**NOTE**

The following conventions are used in this section:
A subscript $_H$ indicates hexadecimal notation and $_D$ indicates decimal notation. An active low signal name is bracketed by slashes /Reset/ = $\overline{\text{Reset}}$.

### 2.1.2 Microprocessor Group

The R6502 microprocessor has the following inputs:

- /Reset/ which is generated at power up by delaying the charging of a capacitor and causes the processor to begin program execution at the address stored at 7FFC and 7FFD$_H$.
- $\phi$ 0 Clock, which it uses to generate the master timing signals.
- /NMI/ (Non Maskable Interrupt) which is the /Data Ready Interrupt/ from the ACIA.
- /IRQ/ (Interrupt Request) which is generated at each vertical retrace (50 or 60 times/second) and causes the processor to scan the keyboard.

The outputs are:

- $\phi$ 2 Clock, which is the $\phi$ 0 Clock delayed, and is used as the master clock for the microprocessor, ACIA and R6531 chips.
- The sixteen bit address bus (A0-A15) (A15 not used).
- The Read/Not Write (R/W) strobe.

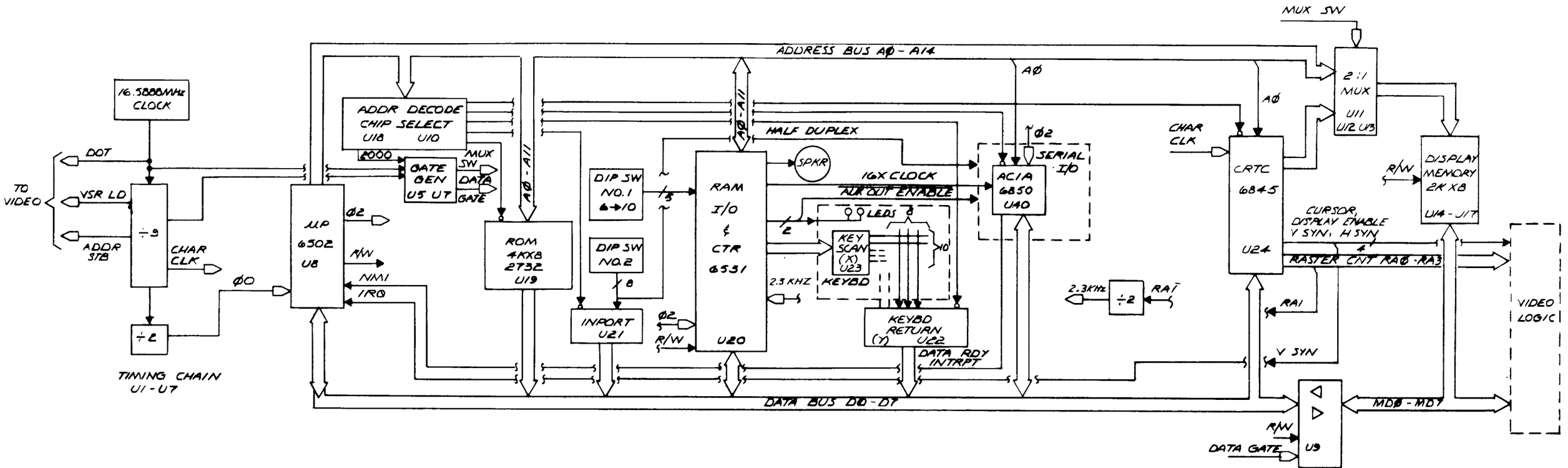
The eight bit data bus (D0-D7) is both input and output.

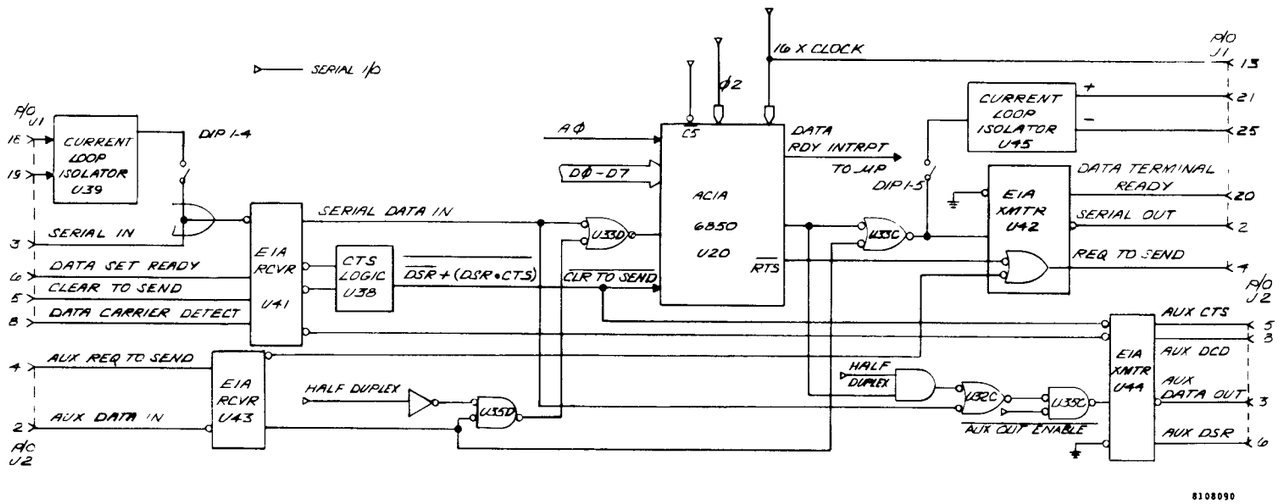
2.1.2.1 **Memory Organization**

The microprocessor has no internal RAM for its stack or scratchpad (temporary storage and flags). The R6531 chip provides 128 bytes of RAM plus counters and I/O ports. To understand the organization of the RAM area it is necessary to know a little about the internal operation of the R6502 microprocessor. It is an 8 bit processor, and although it can handle 16 bit addresses, it must use two bytes to do so. To avoid the necessity of handling 16 bit addresses for every operation, memory is divided into 256 byte "pages" (ie, the largest area which can be addressed by 8 bits). The most significant (high) 8 address bits select one of 256 pages, and the least significant (low) 8 bits select one of 256 bytes from that page. There are a large set of instructions which "assume page 0". Only the low 8 address bits are used and the high address is all 0's. This results in less code and faster operation. In order to make use of these functions it is necessary that the scratchpad area be placed in page 0 (lowest 256 bytes) of the memory map (figure 2-2). Conversely, all stack operations "assume page 1". Only an 8 bit stack pointer is used and the 8 high bits are automatically 00000001. The RAM dedicated to the stack, therefore, must be in page 1 (addr. $100_H$ to $1FF_H$). The R6531 chip has only 128 bytes (1/2 page) of RAM and we wish to have part of it in page 0 and part in page 1. The R6531 chip lets us have it both ways; it ignores address bit A8 ($100_H$) when an address is within its RAM range (but not when it is in the I/O register range). Therefore, an address of $000_H$ or $100_H$ both access the same RAM location (000 through 0FF = 100 through 1FF). Put another way, each byte of RAM in the R6531 chip has two addresses, one on page 0 and one on page 1.

In addition, address bit A7 ($80_H$) is inverted at the input to the R6531 chip. This places the RAM area in the **top** half of page 0 and page 1 as shown in figure 2-2 (address 080 or $180_H$ from the processor become 000 at the R6531 chip). The low 64 bytes are used as a cyclical input queue (paragraph 2.1.2.3) and addressed as page 0. The stack pointer is initialized at the top of page 1 (1FF) and the stack grows downward. The area between the stack and queue is used for flags and temporary storage registers.

This leaves room at the bottom half of page 0 for the peripheral chips, which is convenient because of the way data is down loaded to the CRTC and ACIA. The address decoder/chip select logic (U10, U18) decodes the addresses of the CRTC, the keyboard Y and DIP switch input ports, and the ACIA; and generates the necessary chip select (/CS/) signals. Address bit A0 is applied to the register select inputs of the CRTC and ACIA. To access a register in the CRTC, the processor addresses the device with bit A0 = 0 (not decoded by U10, U18), and outputs the **address** of the desired register on the data bus. With A0 = 0, the CRTC interprets the data on the data bus as a pointer to the register to be accessed. The processor then increments the address output (A0 = 1) and writes to or reads from the selected register.



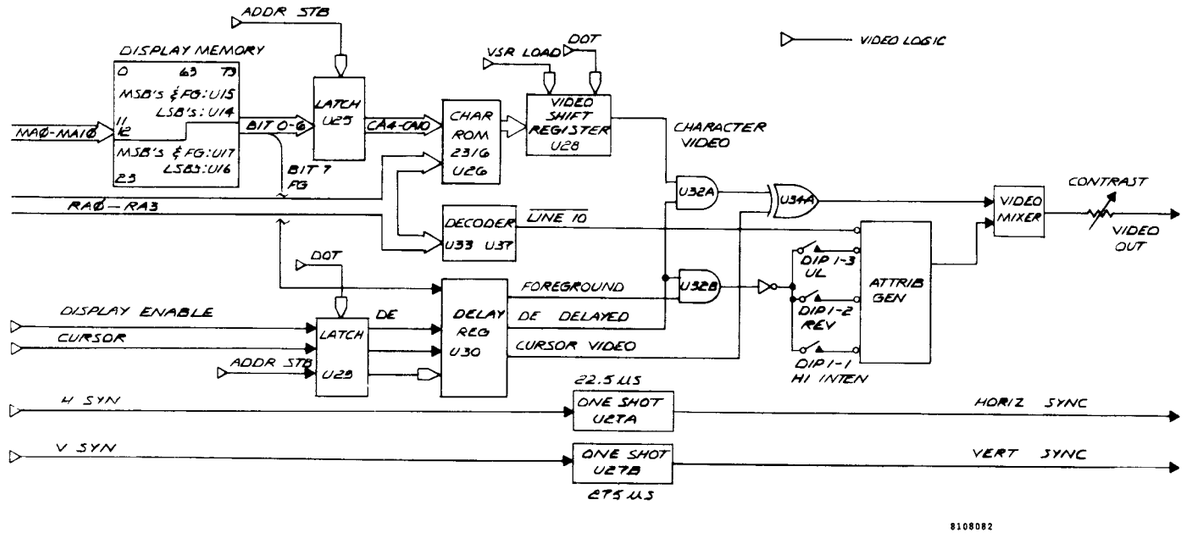




Figure 2-1. **Terminal Block Diagram**

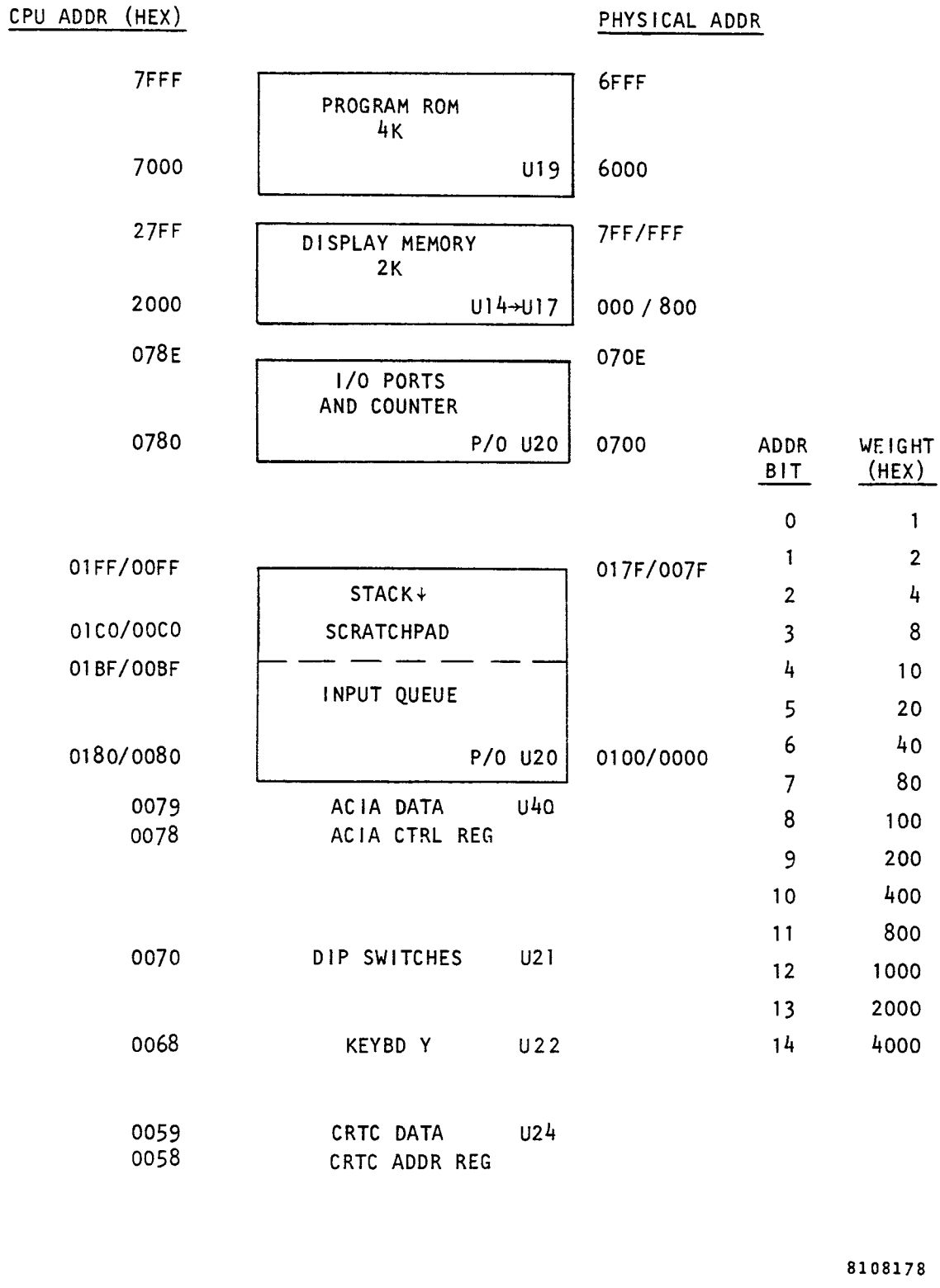



Figure 2-2. **Memory Map**

The I/O ports and control registers in the R6531 chip have addresses in the range 0700 to $070E_H$ (15 registers), but because bit A7 is inverted, must be addressed as 0780 to 078E by the processor. Address bit A13 ($2000_H$) from the processor becomes bit A11 ($800_H$) at the R6531 chip. This prevents the R6531 from responding when the processor addresses display memory ($2000_H$ plus) or program ROM ($7000_H$ plus).

Access to display memory is normally granted to the CRTC (transceiver U9 in high impedance state, multiplexer U11, U12, U13 selecting CRTC MA0 -- MA10, R/W strobe high). When addressed by the CRTC, display memory addresses range from 000 to $7FF_H$ (0 to $2047_D$). Since address bit A11 ($800_H$) is not decoded by display memory, they also range from 800 to $FFF_H$. This characteristic is needed. At turn on or after a "Clear Screen" memory allocations are as shown on figure 2-1. The starting address (top of page) for the top row (No. 0) is 000, No. 1 is $50_H(80_D)$, No. 2 is $A0_H(160_D)$ etc. However, once the cursor reaches the bottom of the display and additional entries cause a rollup (top row deleted from memory) it is not practical (too time consuming) to move all the remaining data in memory so the top of page address remains 000. Instead, a new top of page address is loaded into the CRTC whenever a rollup occurs ($50_H/80_D$ after 1st rollup, $A0_H/160_D$ after 2nd rollup, etc), and the row deleted from the display is cleared to spaces. Figure 2-3 shows the display memory area utilized after two rollups. With a top of page address of $0A0_H$ and 1920 characters displayed, the memory

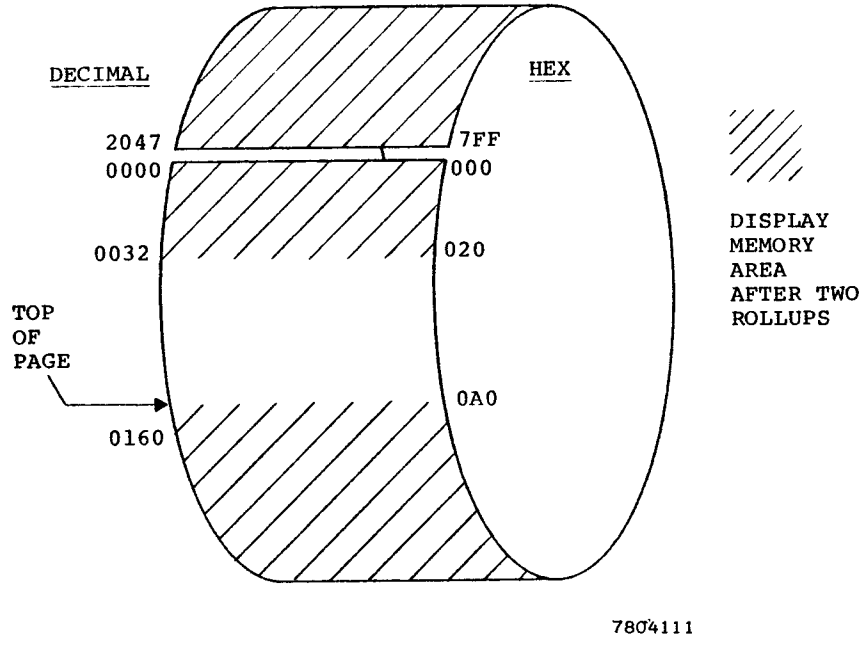



Figure 2-3. **Display Memory Locations After Two Rollups**

addresses will extend beyond the end of memory to $820_H$. However, since bit A11 is not decoded, the data will overflow from 7FF to $000_H$. Because the CRTC is responsible for generating the cursor video when the address being refreshed matches the cursor address, cursor addresses are also allowed to extend beyond $7FF_H$. When the top of page address becomes greater than $77F_H$ the processor adjusts both top of page and cursor addresses (subtracts $800_H$).

When display memory is accessed by the processor its addresses range from 2000 to $27FF_H$. The address decode/chip select logic decodes the high order bits (A13 & /A14/) and the resulting /2XXX/ signal is gated with timing signals (paragraph 2.1.3) to generate the signals which switch the multiplexer to select the microprocessor address bus (instead of the CRTC address outputs), and to enable the data bus to the display memory (Data Gate) via transceiver U9. The R/W strobe controls the direction of data transfer by the transceiver and whether memory is written to or read from.

The program ROM is located at the top of the memory map as shown in figure 2-2. This is necessary because the processor automatically looks to the top of memory for the interrupt and restart vectors. The addresses used in the program are in the $7000_H$ range but bit A12 is not decoded anywhere so the actual addresses are in the $6000_H$ range.

### 2.1.2.2 I/O Ports and Counters

The R6531 chip contains two I/O ports (PA and PB) used for input and output, a counter used to generate the 16 X Baud rate clock for the ACIA, and a serial data channel used to sound key clicks and alarms. Each I/O port bit can be either input or output, but each bit is used in one direction only in this application. The R6531 data direction registers are down loaded during the turn-on initialization sequence to function as follows:

| Port Bit(s) | Direction | Function |
|---|---|---|
| PA0-3 | Out | Keyboard X Scan |
| PA4-7 | In | DIP 1 Switches 7-10 |
| PB0 | Out | /Aux Out Enable/ |
| PB1 | Out | /Block LED/ |
| PB2 | In | Serial Clock Source |
| PB3 | Out | Serial Out (Spkr Drive) |
| PB4 | Out | 16 X Baud Rate Clock |
| PB6 | In | DIP 1-6 |

The control registers are down loaded to configure the 16 bit counter as a free running event counter using the Ø2 clock (921.6 kHz) as the source and producing a pulse output at PB4; and to configure the 8 bit serial data channel to use the leading edge of PB2 as the clock source and to output at PB3. An appropriate 16 bit number (N) is loaded into the R6531 data latches, depending on the baud rate, and the counter produces a pulse output on every Nth Ø 2 clock.

The serial data register is initially loaded with all 1's. This results in continuous high level output and no tone is sounded. To generate a key click the processor loads a pattern of 00001111 into the serial data register. The clock input for the serial channel at PB2 is the second bit ($2^2$) of the raster count output from the CRTC divided by two (simply a convenient source of a signal in the necessary frequency range). The output to the speaker is one pulse period for each eight clock pulses for a 288 Hz tone. To generate an alarm (beep) the processor loads a pattern of 01010101 which produces four pulse periods for each eight clock pulses for a 1.15 kHz tone.

### 2.1.2.3 **Program**

Operation of the terminal is controlled by the program stored in the program ROM. An overview of the program is shown in figure 2-4. At turn on the microprocessor automatically loads the restart vector at 7FFC and 7FFD (actually FFFC and FFFD but address bit A15 is not used in the terminal) into its program counter and begins execution at the address stored there (7E37). This is the initialization routine during which the processor initializes the stack pointer, CRTC, and R6531 and tests ROM (checksum verification), display and scratchpad RAM (read after write) and I/O operation (loopback). It also checks the keyboard but the test is limited to detection of a short or an open cable connection. If any errors are detected an error message will be displayed as described in Section 3. The program then enters the "Set Parameters" phase of initialization where it reads the DIP switches, down loads the Baud rate divisor to the R6531 counter, and the character length, parity and stop bit characteristics to the ACIA, and sets numerous flags and registers in the scratchpad area, most of which relate to how commands are to be handled for the emulation selected. At the end of this sequence the interrupt request is enabled (/IRQ/ is ignored up to this point) and the program enters the main loop, where it remains until interrupted.

Both received and keyboard data are passed to the main loop for processing via a 64 character input queue. The primary purpose of the queue is to permit processing time consuming commands (those which require extensive reading or writing from/to display memory such as clear foreground or insert line) without losing characters or requiring large numbers of fill characters. Received characters are simply allowed to back up in the queue until the processor completes execution of the command.

When the ACIA receives an input character, it generates a data ready interrupt (/NMI/) to the processor.

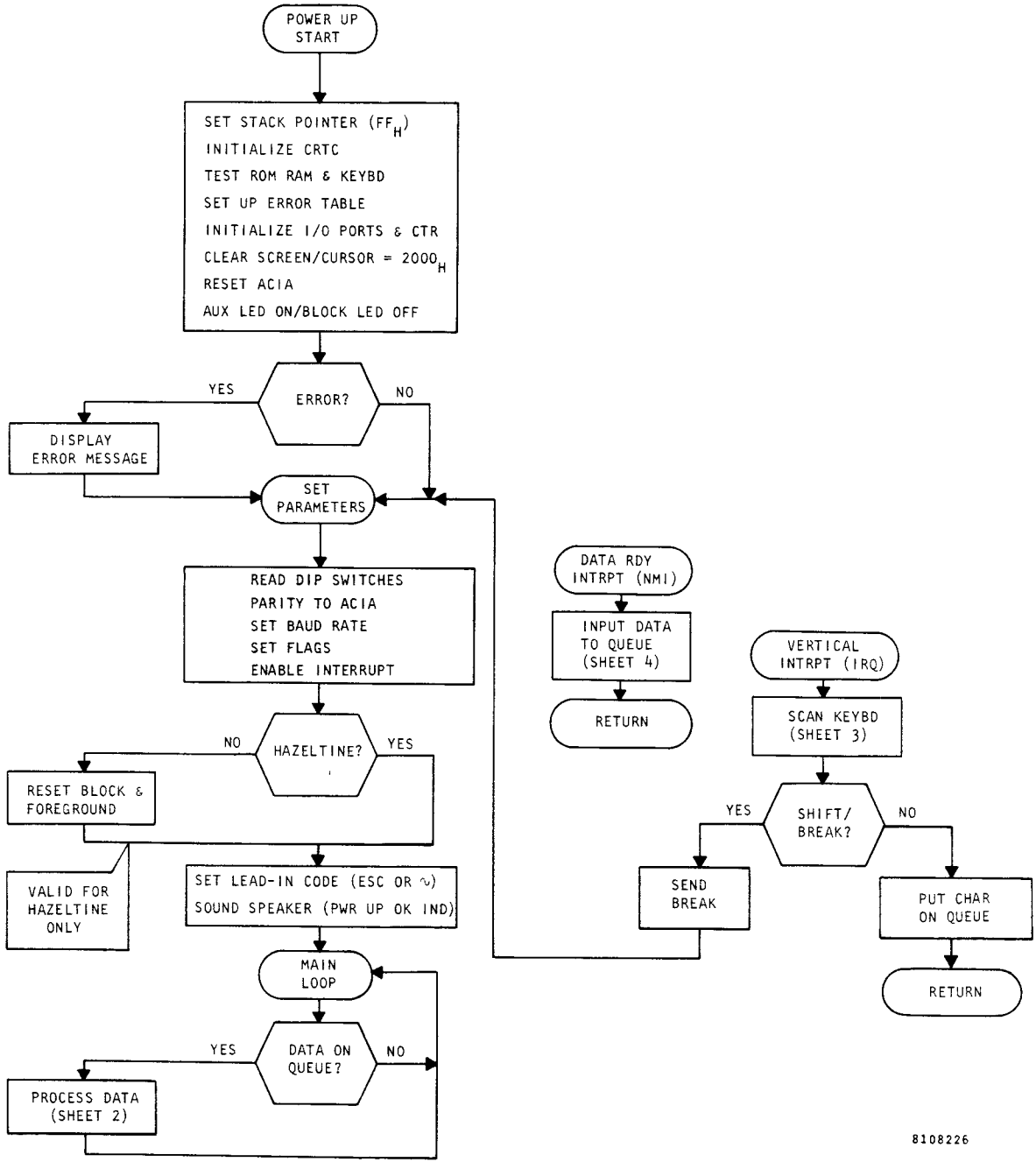



Figure 2-4. **Simplified Program Flowchart** (Sheet 1 of 4)

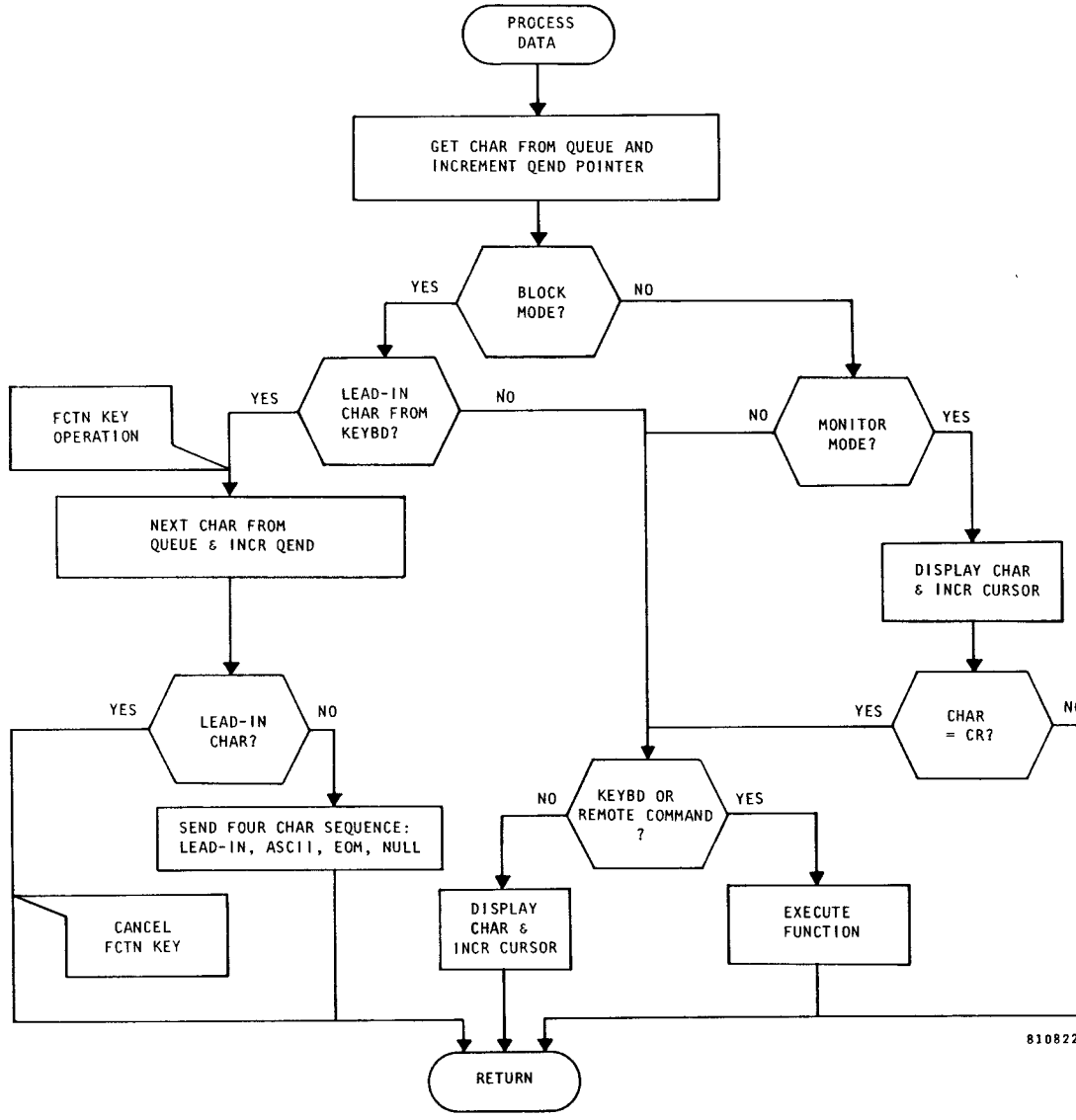



Figure 2-4. **Simplified Program Flowchart** (Sheet 2 of 4)

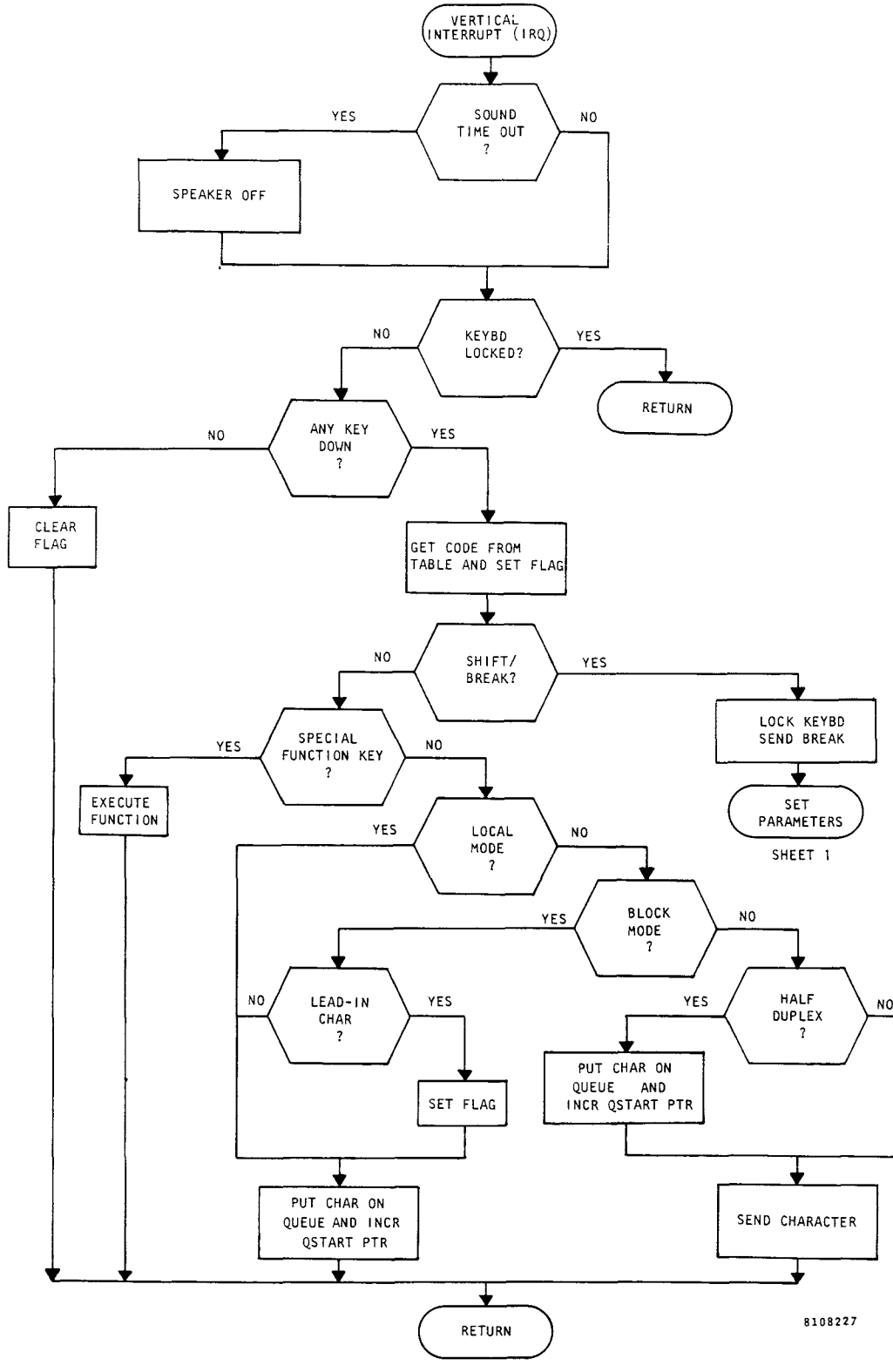



Figure 2-4. **Simplified Program Flowchart** (Sheet 3 of 4)

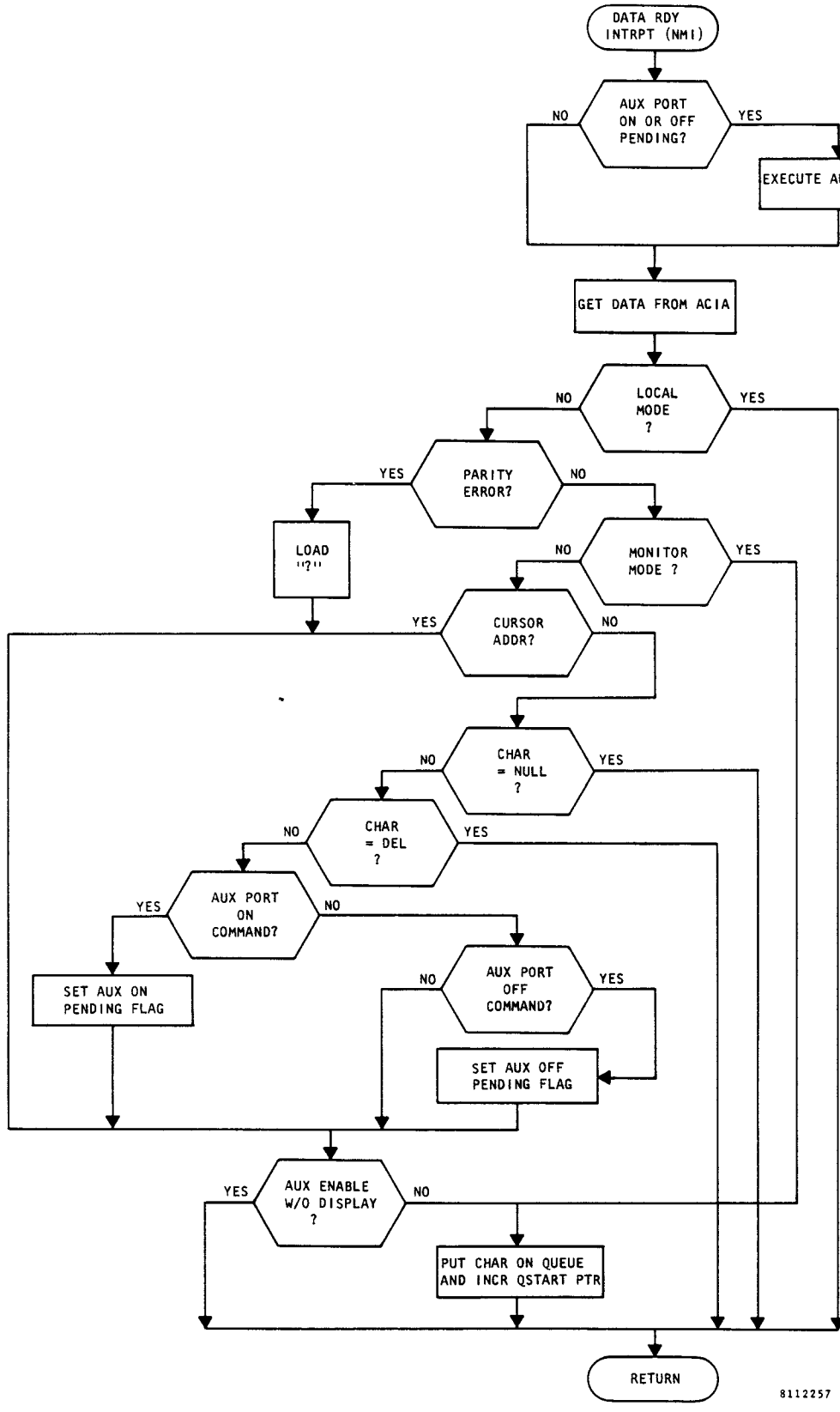



Figure 2-4. **Simplified Program Flowchart** (Sheet 4 of 4)

This causes the processor to push the contents of its program counter and registers onto the stack, decrementing the stack pointer after each byte (the stack grows downward). It then automatically loads the interrupt vector at addresses 7FFA and 7FFB into its program counter and begins execution of the "input data" service routine at the address stored there (755F). This routine results in placing the input character in the next slot on the queue (with some exceptions which require that commands be processed during the interrupt service routine as described later). Control is then "returned" to the main loop. The stack pointer is incremented and the data which was stored in the stack at the start of the interrupt routine is popped back into the registers and program counter and execution is resumed at the point where it was interrupted.

Each time a vertical sync pulse is generated (50 or 60 times/second) an interrupt request (/IRQ/) to the processor is also generated. Handling of the interrupt is as described previously except the interrupt vector is taken from 7FFE and 7FFF and causes execution of the service routine starting at 73DF. This causes the processor to scan the keyboard and, if an entry is detected, the character is placed on the queue and control returned to the main loop (again, with some exceptions described later).

Normally, only the main loop and the two interrupt service routines are executed once the turn on sequence is completed. In order to permit changing DIP switch selections after power up without turning the terminal off, the program re-executes the "Set Parameters" portion of the initialization routine after a break signal. If the Baud rate, parity, EOM, lead-in or emulation switch selections are changed after power up, SHIFT/BREAK must be entered to cause the processor to read the switches and set new parameters.

When the main loop finds that a character is on the queue for processing (QStart pointer not equal to QEnd pointer) it processes the character as shown on sheet 2 of figure 2-4.

The interrupt request service routine is shown on sheet 3 of figure 2-4. The first steps pertain to terminating alarms and key clicks. When an alarm or key click is to be sounded the appropriate subroutine loads the R6531 serial channel to start the sound, and presets an index in scratchpad to control its duration. Each time an interrupt request is serviced the index is decremented, and when it reaches 0 the sound is terminated (all 1's to R6531 serial channel). The keyboard is then scanned by writing a binary 0 to outport PA0-3 which is decoded by U23 on the keyboard causing a low signal on keyboard X line 0, and reading keyboard Y inport U22 (addr. = $0068_H$). Any bit not equal to 1 in the Y return indicates a key down on the X0 line. The process is repeated nine times outputting binary 1 through 9 to scan each of the ten X lines. The flowchart is greatly simplified; there are provisions to detect and ignore multiple keys down or the same key down on successive scans, and to engage the typamatic feature when a key is held down. When a valid keystroke

is detected the processor uses the X and Y coordinates as the key to one of two lookup tables (depending on whether the SHIFT key is down or not) in ROM to get the corresponding character code.

The "input data" service routine is shown on sheet 4 of figure 2-4. Most input characters are read from the ACIA and placed on the queue for processing by the main loop. Auxiliary out enable and disable commands cannot be handled in this manner for two reasons: (1) if the queue is backed up when the command is received, additional characters could be input before the command is processed and executed, resulting in failure to output them to the auxiliary device or in outputting unwanted characters; (2) the auxiliary output could be enabled while a serial character is being received, resulting in part of the character being output. The auxiliary device would interpret the first 0 it sees as a start bit and get garbled data. Therefore, these commands are executed in the input service routine. When a lead-in character is received a flag is set. With the flag set the input service routine checks the next character to see if it is an aux on or aux off command, and clears the flag. If it is an aux off or aux on command an "aux pending" flag is set. With this flag set, the aux output will be enabled or disabled immediately upon recept of the **next** character, insuring that it is not turned on while a character is being received. Note that this requires "wasting" one character after an aux command.

In order to permit killing time without filling the input queue while the processor executes a time consuming command, NUL and DEL characters are not placed on the queue, except for Regent 25 emulation, where NUL is accepted, or when part of a Hazeltine direct cursor address sequence.

### 2.1.3 Timing

Timing signals for both the processor group and the CRTC/ Character Generator circuits are provided by the same timing chain to prevent contention between the two functions for display memory access. The 16.5888 MHz crystal oscillator provides the dot clock to the video shift register and is the basis for all other timing signals. The basic timing relationships are shown in figure 2-5. As the dot pattern for the character currently being refreshed is being clocked out of the video shift register by the dot clock, the next character code from the display memory location addressed by the CRTC is latched into U25 by the address strobe. This data, in conjunction with the raster line count from the CRTC selects the dot pattern of a particular TV line of the character font in the character generator ROM (figure 1-4). At the start of the next character window the VSR Load signal enables the dot pattern to be loaded into the video shift register. The O0 clock input to the CPU is at one half the character clock rate. It is a characteristic of the R6502 microprocessor that it reads or writes from or to memory only during the last quarter of a

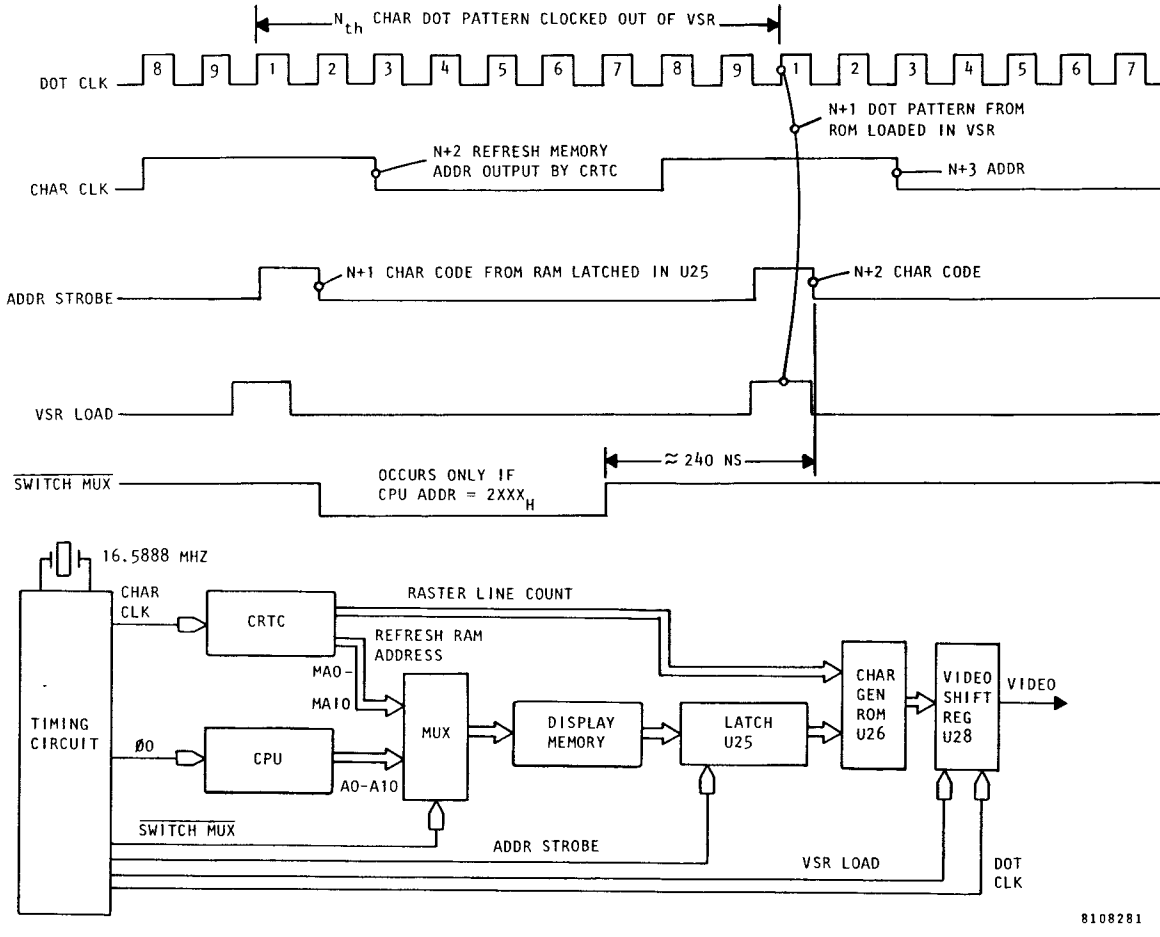



Figure 2-5. **Basic Timing Relationships**

clock cycle. By tying the ∅0 clock to the character clock we insure a fixed relationship between CPU read/write timing and character timing. When the processor outputs an address in the display memory range ($2XXX_H$) the decoded high order bits are gated with a timing signal (∅4) and the /SWITCH MUX/ signal generated as shown in figure 2-5. The multiplexer puts the CPU address on the bus at a time when the CRTC address for the current character has been latched into U25, and puts the next CRTC address back on the bus in time for data to be stable at the latch input when the next address strobe occurs.

### 2.1.4 CRTC and Character Generator

Synchronization and refresh of the TV display are contnrolled by the CRTC (figure 2-1) based on parameters down loaded to its registers during the turn-on initialization sequence. The initial values are:

| | |
|---|---|
| Characters/Line (total) | 100 |
| Horizontal Chars Displayed | 80 |
| H Sync Position (Char No.) | 80 |
| H Sync Width (Chars) | 10 |
| Vertical Total Lines (60Hz) | 307 |
| Vertical Total Lines (50Hz) | 369 |
| Vertical Display (Rows) | 24 |
| V Sync (Row No.) (60Hz) | 24-7/12 |
| V Sync (Row No.) (50Hz) | 29-9/12 |
| Interlace | No |
| Raster Lines/Row | 12 |
| Cursor - Blink | No |
| - Start Line | 0 |
| - End Line | 11 |
| Cursor Address | 000 |
| Display Start Address | 000 |

This results in a non blinking block cursor at the home position. The cursor characteristics are changed by the processor when the operator selects a different cursor representation. The cursor address is changed every time the cursor is moved, and the start address is changed whenever a rollup occurs (paragraph 2.1.2.1).

The character clock (dot clock/9 = 16.5888 MHz/9 = 1.843 MHz (542.6 ns)) input to the CRT serves as the basis of all CRT timing. The horizontal character display and vertical row display are chosen to generate the desired 80 x 24 display format. The horizontal total and H sync position are chosen to accommodate the requirements of the TV monitor and allow time for horizontal flyback. The H sync width is arbitrary, the maximum programmable width (15 chars) is too short for the monitor and is stretched to 22.5 microseconds by one shot U27A. The V sync output from the CRTC triggers 275 microsecond one shot U27B to generate the vertical sync signal used by the monitor. The vertical total is chosen to make the refresh rate equal to 50 or 60 Hz as follows:

1.848 MHz (char clk)/100 char per line = 18.48 kHz (horiz freq)
18.48 kHz/307 lines per frame = 60 frames/s
18.48 kHz/369 lines per frame = 50 frames/s

It is important that the refresh rate be an integral fraction of the line frequency to minimize the effect of power supply ripple on the display.

Starting at the top of the display area, the CRTC outputs a memory address equal to the display start address, and a 4 bit raster count equal to 0. The address output is incremented on each character clock for 80 consecutive characters. This causes the eighty 80 character codes to be read from display memory and latched into U25 where they address the corresponding character font in the character generator ROM (figure 1-4). After 80 characters have been accessed, H sync is generated and the Display Enable signal goes low, blanking the video during flyback. An additional 20 character clocks are counted to allow time for horizontal flyback and the raster count is incremented to 1. Display enable then goes high and the same 80 addresses are output again to generate the second TV line of the top

character row. This process is repeated until all twelve TV lines of the top row have been generated. The CRTC then resets the raster count to 0 and outputs addresses beginning with the start address plus 80 to generate the second row of characters. After all 24 rows have been refreshed the V sync signal is generated and display enable held low to blank the video during vertical retrace. The CRTC counts additional TV lines up to the specified vertical total (307 or 369) to allow time for vertical retrace and then repeats the cycle.

When the address currently being output matches the cursor address the CRTC generates the cursor signal for all 12 raster counts if a block cursor is selected, or on line 11 only if an underline cursor is selected. If a blinking cursor is selected the cursor output is omitted for 8 of each 16 frames (fast) or 16 of each 32 frames (slow).

Each byte in display memory contains the seven bit ASCII code for the character at that location. The eighth bit is a 1 for foreground characters and a 0 for background characters. When the ASCII code is latched into U25 to address the character font, bit 7 (FG) is held in delay register U30 along with the Display Enable and Cursor signals from the CRTC. As shown on figure 2-5, there is a 1 character delay between the time a character is read from display memory and the time the dot pattern is loaded into the video shift register. The delayed FG bit is applied to those portions of the attribute generator logic selected by the DIP switches. If underline is selected an under-line is generated on line 10. If reverse video is selected the entire character window is reversed. If high intensity is selected the video is intensified at the output. The delayed Display Enable bit must be present to permit video to be gated through U32A. The cursor signal is mixed with the character video at Exclusive OR gate U34A. This causes a reverse video representation of the character video when the cursor signal is present.

The video shift register is an 8 bit recirculating register. Since it is clocked nine times per character, the 9th bit is equal to the first bit recirculated (both always 0).

### 2.1.5 **Serial I/O**

The central element of the serial I/O logic (figure 2-1) is the MC 6850 Asynchronous Communications Interface Adapter. The ACIA has four registers addressible by the processor via the chip select, register select (addr. bit A0) and R/W strobe:

| A0 | Register (Read) | Register (Write) |
|---|---|---|
| 0 | Received Data | Transmit Data |
| 1 | Status | Control |

The control register is down loaded during the turn-on initialization sequence for a seven bit character plus odd or even parity (depending upon DIP switch selection) and one or two stop bits (110 Baud); or for an eight bit character, no parity and one or two stop bits. When set for seven bits plus parity the ACIA formats transmit data as, start bit, 7 bit character code (data bit D7 is ignored), parity bit, 1 or 2 stop bits, and transmits it serially at the Baud rate determined by the 16X clock. For received data it strips the start and stop bits, checks parity, loads the 7 bit character into the received data register (bit D7 will be 0), and interrupts the processor. If a parity error is detected it is indicated by a bit in the control register. The processor then reads the data register to get the received character and the control register to determine if a parity error was detected. Operation is similar when parity bit = 0 or 1 is selected except the processor inserts the selected parity bit as data bit D7, and the ACIA transmits the eight bits plus start and stop bits. No parity check is made by the ACIA and a parity error is never indicated. The ACIA also raises and drops the Request to Send output based on the command loaded in its control register, and indicates the presence or absence of "Clear to Send" in its status register. If /Clear to Send/ is not present at the ACIA, the "Transmitter Holding Register Empty" bit in its register will not be set. Note that this input at the ACIA is not the "Clear to Send" control signal at the EIA input. The control signal is gated with the "Data Set Ready" input so that /Clear to Send/ will be true (low) if the "Clear to Send" control signal is true or if the "Data Set Ready" control signal is false (ie, if there is no Data Set Ready it is assumed that the modem control protocol is not to be observed, as in a hard wired interface for example, and the terminal transmits regardless of the state of the Clear to Send line. The Data Terminal Ready signal from the terminal is hard wired and will be true (high) whenever power is on.

The serial data input to the ACIA may be from the primary EIA line (J1 pin 2), the current loop receiver, or, in half duplex only, the auxiliary input (J2 pin 3). The transmitted data may be output at the primary EIA line (J1 pin 2), the current loop transmitter, and if in half duplex with aux out enabled, the auxiliary output line (J2 pin 3). Note that the transmit and receive data pins are interchanged at the auxiliary port connector (compared to the primary connector) so it looks like a Data Communication Device and can be connected pin for pin to a Data Terminal Device.

The Data Carrier Detect input at the primary EIA connector is relayed to the auxiliary output and the Auxiliary Request to Send is relayed to the primary EIA output; neither signal is used in the terminal.

Both primary and auxiliary output signals are converted from TTL levels to EIA levels by the EIA transmitters (U42 or U44):

| | | TTL | EIA |
|---|---|---|---|
| Data | 1 | 2.4 to 5 v | -10 v |
| | 0 | 0 to 0.4 v | +10 v |
| Ctrl | True | 0 to 0.4 v | +10 v |
| | False | 2.4 to 5 v | -10 v |

Received EIA signals are converted to TTL levels by EIA receivers (U41 or U43). Received EIA levels may range from +3.5 to +25 vdc and -3.5 to -25 vdc. Note also that EIA data lines idle in the "mark" state; if there is no data being input or output the serial data lines should be at 2.4 to 5 v on the TTL side of the logic.

## 2.2 TV MONITOR

### 2.2.1 Introduction

The TV monitor (figure 2-6) consists of the CRT, yoke coils and monitor circuit board. The monitor circuit board contains the video amplifier, which drives the CRT cathode; the vertical and horizontal deflection circuits, which are synchronized to the vertical and horizontal sync pulses from the main logic board; and the flyback transformer, which generates high voltages for the CRT electrodes and 70-volt B+ for the video amplifier.

### 2.2.2 Video Amplifier

The video amplifier is a two stage cascode configuration (figure C-3). Q101 is permanently biased on by the 6.2 volts established by Zener diode D101. With no video input (less than 0.4 volts) Q102 does not conduct. The video signal (approx. 4 volts for full brightness) is coupled to the base of Q102 by R101 and causes it to conduct. The peaking circuit on the emitter of Q101 (R103, R104, C102) compensates for the difference in

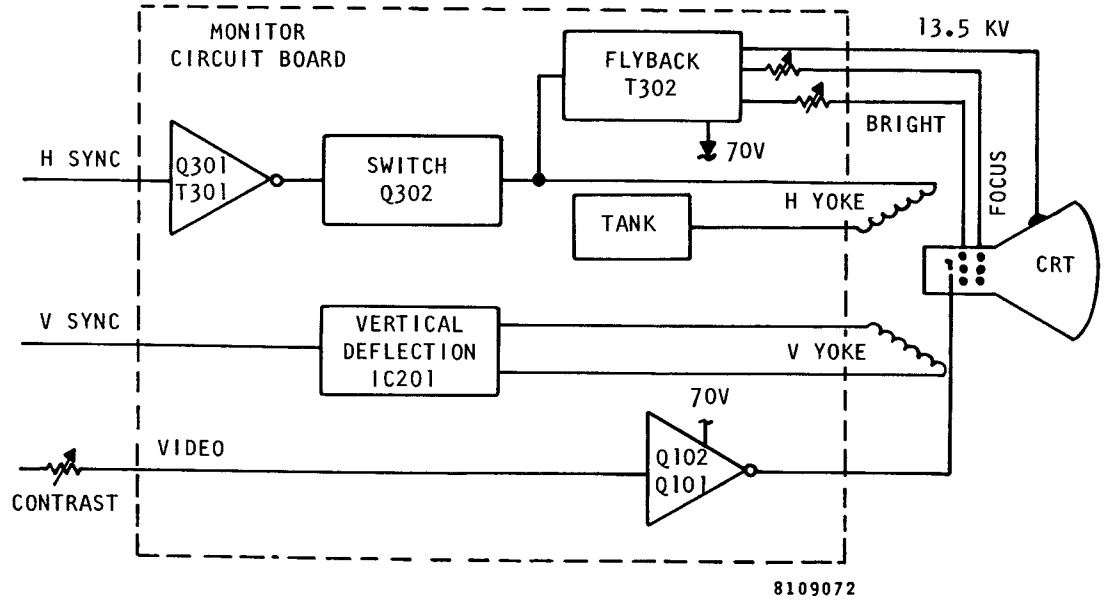



Figure 2-6. **Monitor Block Diagram**

brightness that would otherwise occur between a single dot pulse (as in the vertical stroke of a T) and a horizontal stroke (as in the cross of a T). The amplified and inverted video output is coupled to the cathode by L101, which boosts high frequency response, and R106, which isolates Q101 from transients which may occur as a result of arcing in the CRT. C103 bypasses any AC component in the 70 volt source and C101 prevents any high frequency signal from appearing at the base of Q101.

### 2.2.3 Horizontal Deflection Circuit

The horizontal deflectioncircuit consists of predrive Q301/T301, output switch Q302/D301, and a tank circuit which includes the horizontal yoke coil. As deflection begins at the left side of the CRT, energy stored in the yoke is discharged through a loop formed by the yoke, linearity coil, width coil and damper diode D301. The current diminishes, reaching zero near the center of the sweep. Q302 is switched into conduction slightly before deflection reaches the center of the screen. During the right half of the scan, energy stored in C303 is discharged through Q302, the width and linearity coils and the yoke coil. When the scan reaches the right side of the screen, the leading edge of the vertical sync pulse is coupled to the base of Q302 by the predriver. Q301 goes into saturation and Q302 is cut off. R303 and C301 provide damping to prevent ringing in the primary of T301 when Q301 is cut off and R302 limits current through Q301. When Q302 is cut off the yoke current is abruptly interrupted, producing ringing in the tank circuit as the inductive field collapses. Yoke current reverses, causing rapid deflection of the beam to the left side (flyback). The ringing is limited to one positive excursion by D301 as the diode conducts when the voltage attempts to go negative. The voltage pulse charges C303 and the cycle repeats.

### 2.2.4 Electrode Voltages

The rapid voltage fluctuations in the horizontal deflection circuit are also applied to the primary of flyback transformer T302. The flyback transformer develops the 13.5 kv anode voltage through an internal diode, approximately 550 volts for the focus and control grids via D306 and C307, +70 vdc for the video amplifier via D304 and C308, and + and - 70 volts for the brightness circuit.

### 2.2.5 Vertical Deflection Circuit

Current through the vertical yoke coil is controlled by vertical deflection generator IC201. The circuit is shown in figure 2-7. The oscillator frequency is adjusted by VR201 to slightly less than the vertical sync rate (ie, it will free-run at a slightly slower rate than the TV vertical refresh rate). The oscillator triggers a ramp generator which generates a ramp function. The slope of the ramp, and thereby the display height, is controlled by VR202. The ramp output is given an S shape in a buffer stage which includes linearity control VR203, to better conform to the geometry of the CRT. The buffer output, along with a feedback signal via R212, is amplified in two stages. The feedback compensates for temperature related changes in yoke coil

resistance. The output at pin 4 is applied to C212 to control current flow through the yoke coil. R209 and R203 establish the centerline or undriven voltage level at pin 4. When the vertical sync pulse is received, the oscillator is retriggered and the ramp generator is reset. At this point, the flyback generator triggers a large voltage pulse at pin 4 which causes vertical retrace to the top of the screen.

## 2.3 POWER SUPPLY

### 2.3.1 Introduction

The power supply circuit board (figure C-4) contains separate regulators for +5 vdc, +15 vdc and -12 vdc. The +12 vdc for the EIA drivers is derived from the +15 vdc supply by Zener diode D4 on the main logic board.

### 2.3.2 Plus 5 Volt Regulator.

AC voltage from the secondary of the power transformer is rectified by bridge D50 to provide approximately +12 vdc across filter capacitor C50. This is dropped to approximately 11 volts at the input to 5 volt regulator U50. U50 regulates the output voltage at +5 volts which is filtered by C62, C59 and C53. The drop across R51 is sufficient to cause Q51 to conduct, shunting most of the current around the regulator chip U50. If an over-current condition occurs the drop across R53 will cause Q53 to conduct, reducing the emitter to base difference at Q51 and reducing the current output.

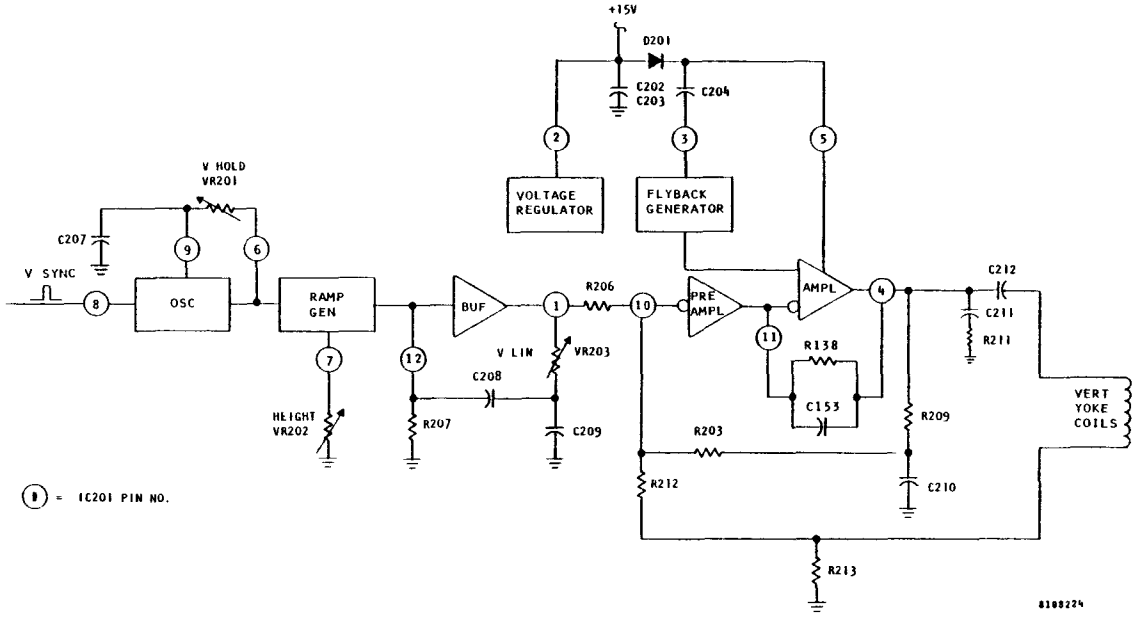



Figure 2-7. **Vertical Deflection Circuit**

### 2.3.3 Plus 15 Volt Regulator

The 15 volt regulator is functionally identical to the 5 volt regulator. The dc voltage across C51 is approximately +27 volts and a 15 volt regulator chip (U52) is used.

### 2.3.4 Minus 12 Volt Regulator

The current drain in on the -12 volt supply is low enough (only the EIA drivers use it) to permit the regulator chip (U51) to handle it without a current bypass. The ac input is rectified by D52 to produce approximately -21 volts across C52 and C58. This is used to produce a regulated -12 volt output by U51.

# SECTION 3

# MAINTENANCE

## 3.1 SCOPE

This section provides checkout and troubleshooting procedures to both the circuit board and component levels.

## 3.2 CHECKOUT

### 3.2.1 Setup and Self Test

a. Set the DIP switches at the rear of the terminal as follows:

10 Switch DIP 1

| | |
|---|---|
| 1 | ON Hi Inten |
| 2 | ON Rev Vid |
| 3 | ON U Line |
| 4, 5 | ON if EIA, Off if I Loop |
| 6 | ON ESC |
| 7, 8 | ON Hazeltine |

8 Switch DIP 2

| | |
|---|---|
| 6 | ON Auto NL |
| 7 | ON Half Dupl |
| 8 | ON Auto LF |

b. Set the POWER switch to ON. The terminal should sound a short beep. The POWER and AUX LED's should be on and the BLOCK LED should be off. After a brief warmup, the steady block cursor should appear at the home position and the screen should be clear with no error message.

At turn-on the terminal automatically runs the following tests:

- Program ROM is checked by reading each word, accumulating a total, and comparing it with a checksum stored in ROM.
- Scratchpad memory is tested by writing patterns of 1's and 0's to each location, and checking that the correct data is read back.
- Display memory is checked in the same manner.
- A test is made for keyboard shorts by reading the return (Y) lines with no X input (all X lines high). If the return is not all 1's, an error message is generated indicating a short in the keyboard or cable.

If an error is detected during self test, the word "ERROR" and one character indicating the fault(s) are displayed. Refer to table 3-1 for the meaning of the error messages.

### 3.2.2 Video Test

**NOTE**

Superscript $^{c}$ and $^{s}$ are used throughout this manual to indicate holding the CTRL and/or SHIFT key down while depressing another key.

Table 3-1. Self Test Error Messages

| Error Character Displayed | | | | | | | | | | | | | | | Fault Detected |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | : | ; | < | = | > | ? | |
| * | | * | | * | | * | | * | | * | | * | | * | Display Memory |
| | * | | | | * | * | | | * | * | | | * | * | Scratchpad |
| | | | * | * | * | * | | | | | * | * | * | * | Program ROM |
| | | | | | | | * | * | * | * | * | * | * | * | Keyboard |

a. Enter $^{S}$LOCAL. The BLOCK LED should blink.

b. Enter $^{C}$4 to enable keyclick.

c. Enter $^{C}$0. A keyclick should sound and the display should fill with low intensity U's.

d. Check display size and centering. Nominal dimensions are 8 inches (20.5 cm) wide by 5.1 inches (13 cm) high.

e. Enter $^{C}$0 again. The screen should fill with underlined *'s in high intensity reverse video.

f. Set DIP 1 switch 1 to off. Display should be low intensity.

g. Set DIP 1 switch 2 to off. Display should revert to normal video.

h. Set DIP 1 switch 3 to off. Underlines should disappear.

### 3.2.3 Character Generator Test

a. Enter ESC 8. Each of the 128 ASCII characters should be displayed in order (Appendix A).

b. Enter $^{C}$CLEAR. The screen should clear.

### 3.2.4 Serial I/O Test

a. Connect a jumper adapter, figure 3-1, to the EIA connector with all switches open. Either the EIA or current loop adapter may be used, or the test may be performed once for each (set DIP 1 switches 4 and 5 to agree).

b. Enter $^{S}$LOCAL. The BLOCK LED should go out.

c. Type any character. The character should appear on the display.

d. Close the CC and Loop switches.

e. Type any character. It should not appear on the display and the key click should not terminate.

f. Close the CB switch. The character typed in step e should be displayed twice, and the key click should terminate.

g. Set DIP 2 switch 7 to off (full duplex).

h. Enter $^{S}$BLOCK. The BLOCK LED should go on.

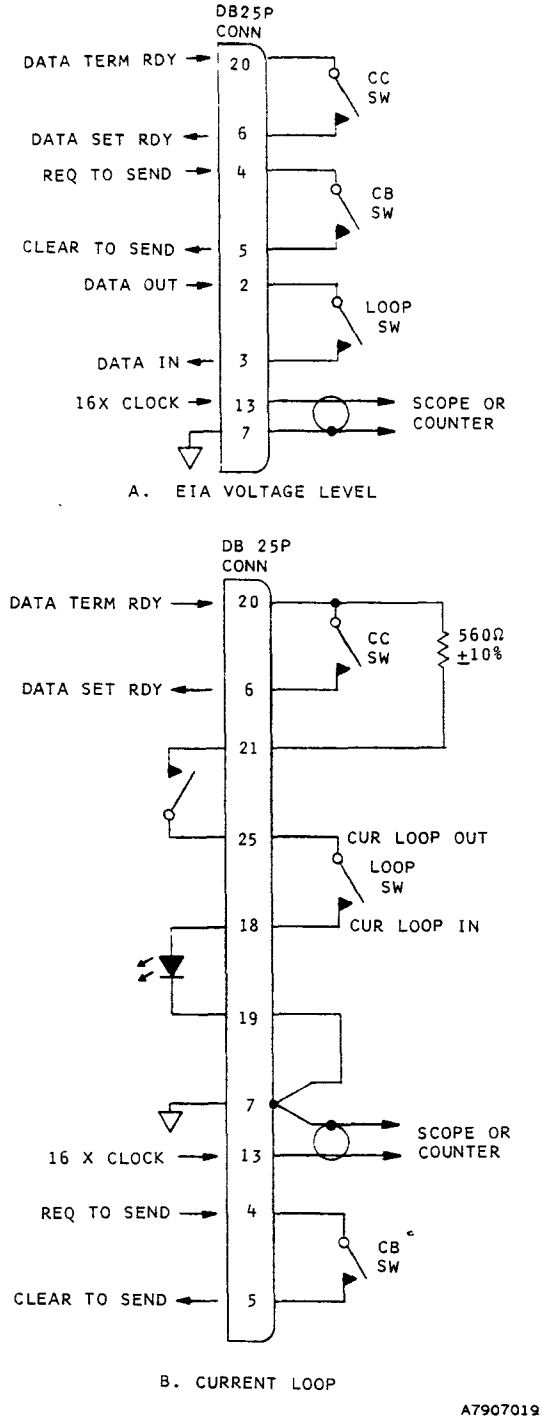



Figure 3-1. Jumper Adapters

i. Enter $^{c}3$ (line mode).

j. Type several characters followed by RETURN. The character string should be repeated on the display.

**NOTE**

Because the same clock is used for both transmit and receive, the previous test does not confirm proper Baud rate. To check Baud rate, another device must be used to communicate with the terminal, or an oscilloscope or counter used (refer to paragraph 3.2.8).

k. Enter BLOCK (OFF). The BLOCK LED should go out.

### 3.2.5 CRTC Check

a. Enter the following and check for the proper cursor representation:

| | |
|---|---|
| $^{c}6$ | Slow Blinking Block |
| $^{c}9$ | Slow Blinking Underline |
| $^{c}7$ | Fast Blinking Underline |
| $^{c}5$ | Static Underline |
| $^{c}8$ | Static Block |

b. Enter $^{s}$HOME. The cursor should home.

c. Enter LINE/INS until the data on the display moves to the bottom half of the screen.

d. Enter $^{s}$DEL/LINE until the data moves back to the top half of the display.

e. Hold the RETURN key down. The cursor should move to the bottom of the screen and all data should scroll up off the display.

### 3.2.6 Aux I/O Check

a. Connect an EIA jumper adapter (A, figure 3-1) to the Aux I/O connector with the Loop switch closed.

b. Set DIP 2 switch 7 to ON (half duplex).

c. Type any character. The character should be displayed twice.

d. Enter AUX/OFF. The AUX LED should go out.

e. Type any character. The character should be displayed once.

### 3.2.7 Keyboard Test

a. Type $^{C}1$ (Monitor Mode).

b. Type $^{CS}2$. $N_U$ should be displayed.

c. Type each character key and check that the appropriate ASCII character is displayed (Appendix A). RUB OUT should cause a block to be displayed.

d. Enter each of the editing keys. The appropriate remote command sequence (Appendix B) should be displayed (e.g., $^{S}$HOME causes $E_CD_2$ to be displayed).

e. Depress the CAPS LOCK key. The key should lock down and alpha keys produce upper case.

### 3.2.8 Baud Rate Check

a. Connect an oscilloscope or counter to pin 13 of the EIA connector.

b. Select each Baud rate in turn by DIP 2 switches 1, 2, and 3; enter $^{S}$BREAK (the terminal should sound a beep) and check for the frequency or period listed in table 3-2.

Table 3-2. 16 times Baud Rates

| Baud Rate | Frequency (kHz) | Period (microseconds) |
|---|---|---|
| 9600 | 151.3 to 155.9 | 6.41 to 6.61 |
| 4800 | 75.65 to 77.9 | 12.8 to 13.2 |
| 3600 | 56.74 to 58.47 | 17.1 to 17.6 |
| 2400 | 37.82 to 38.97 | 25.7 to 26.4 |
| 1200 | 18.91 to 19.49 | 51.3 to 52.8 |
| 600 | 9.456 to 9.744 | 102.6 to 105.7 |
| 300 | 4.728 to 4.872 | 205 to 211 |
| 110 | 1.734 to 1.786 | 560 to 576 |

## 3.3 SERVICING

### 3.3.1 Access

**WARNING**

Dangerous voltages (13,500 vdc, 600 vdc and 100 to 240 vac) are present in the Video Display Terminal. Some voltage may remain present in the monitor circuits after power is disconnected. Use caution when working on the interior of the terminal. Do not work alone.

Use caution when handling the cathode-ray tube (eg, wear safety goggles) to avoid risk of implosion. The internal phosphor coating is toxic; if the tube breaks and skin or eyes are exposed to phosphor, rinse with water immediately and consult a physician.

To gain access to the internal components, release the six screws securing the cover to the base, stand the terminal upright, and lift the cover off the base.

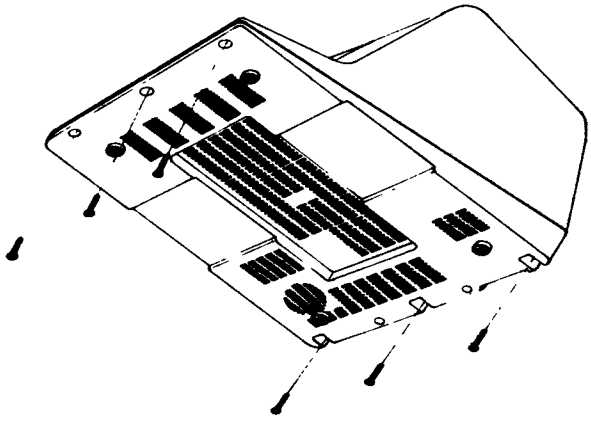


Figure 3-2. Terminal Bottom View

### 3.3.2 Logic Board Removal

a. Disconnect P3 and P5 at the left rear of the board.

b. Disconnect P6 (power supply cable).

c. Lift the rear edge of the board about 1 inch and slide it a few inches toward the rear of the terminal.

d. Disconnect keyboard connector P4 from the DIP socket at the front of the logic board.

e. Slide the logic board out of the terminal.

### 3.3.3 Logic Board Installation

Reverse the procedure of paragraph 3.3.2 taking care that the slides at the sides of the board engage the tracks in the chassis brackets.

### 3.3.4 Monitor Board Removal

a. Disconnect the anode lead from the CRT by pulling straight out on the round plastic cup, and immediately discharging the lead to the chassis brackets by inserting a metal screwdriver or other tool into the cup while the tool is grounded to the chassis.

b. Disconnect logic board connector P1 from the edge of the monitor board.

c. Release the small screw and nut securing the ground wire to the bracket immediately above the connector.

d. Release the two nuts securing the plastic monitor board retainer immediately below the connector.

e. Disconnect the ground wire coming from the CRT from the monitor board by pulling the lug from the tab.

f. Disconnect the two 2-pin connectors labled V Yoke and H Yoke.

g. Disconnect the CRT socket from the tube.

h. Slide the monitor board out of the brackets.

### 3.3.5 Monitor Board Installation

Reverse the procedure of paragraph 3.3.4 taking care to observe polarity on the V Yoke and H Yoke connections.

### 3.3.6 Monitor Alignment

In general, the order in which monitor adjustments are made is not important. The following sequence is recommended, however.

a. Set DIP 2 switches 7 and 8 ON, and turn on the terminal.

b. Adjust contrast control until cursor is visible.

c. Adjust brightness control VR300 until the raster is just visible, and then until it just disappears. (This adjustment is best made within a few minutes of cold turn-on).

d. Type lead-in ( ∿ or ESC) and ". The screen should fill with H's.

e. Set vertical hold control VR201 halfway between the points at which the display rolls up and rolls down.

f. Adjust height control VR202 for a 5.1 inch (13 cm) high display.

g. Adjust width control L302 for an 8 inch (20.5 cm) wide display.

h. Adjust vertical linearity control VR203 for best uniformity of character height over the display.

i. If necessary, adjust the two centering tabs on the CRT neck to center the display.

j. Enter $^{c}$CLEAR to clear the screen.

k. Use the cursor control keys to place the cursor at row 7, column 20 (approximately).

l. Enter $^{c}$1 (monitor mode) and RUB OUT to display a block at the cursor location.

m. Enter $^{c}$2 (cancel monitor mode).

n. Move the cursor to the following locations (approximately) and repeat steps l and m to display a block at each location:

| Row | Column |
|---|---|
| 7 | 60 |
| 15 | 20 |
| 15 | 60 |

o. Adjust focus control VR301 for best overall focus of the four blocks. This adjustment is best made under the same lighting conditions and contrast setting as the terminal will be used with.

### 3.3.7 Keyswitch Replacement

Individual keyswitches on the keyboard may be replaced as follows:

NOTE

The solder side of the keyboard is stencilled with the coordinates of each key. Eg., the CTRL key solder pad (Y = 1, X = 9) is labled 19.

a. Unsolder the two switch contacts from the board.

b. Remove the key cap by pulling straight up.

c. Pinch the two levers at the top of the keyswitch together with a pair of pliers, and pull the body of the switch out of the keyboard.

d. Orient the replacement keyswitch so the legs will align with the solder pads, and press it into the keyboard.

e. Solder the keyswitch to the board.

f. Press the keycap onto the switch actuator.

## 3.4 TROUBLESHOOTING

### 3.4.1 Introduction

A thorough knowledge of the principles of operation described in section 2 is the most important asset in troubleshooting the terminal. Some specific guidelines are given in the following paragraphs.

### 3.4.2 Terminal

Refer to table 3-3 for general troubleshooting information.

Table 3-3. Troubleshooting Chart

| Trouble | Probable Cause |
|---|---|
| No raster, no keyboard response, power OK | U24 |
| Some keyboard characters wrong or no entry | Ref. to para. 3.4.4 |
| Local operation OK, terminal locks up when first transmittable character is entered | U40 |
| Transmit data OK, aux out bad | U44 |
| Bad transmit data, aux out OK | U42 (EIA), U45 (I Loop) |
| No foreground or no background | U29, U30, U32, U37 |
| Constant reverse video or no reverse video | U37, U34 |
| Wrong or broken characters on both top and bottom half of display; vertical lines | U26, U28 |
| Wrong characters in part of display | Refer to para. 3.4.3 |
| No cursor, characters OK | U24, U29, U30 |

### 3.4.3 Display Memory

If self test or operation indicates a display memory fault, the problem can be further isolated with the built-in-test patterns. At turn on, display memory is organized as follows:

| | Top 1024 Character (12.6 rows) | Bottom 896 Character |
|---|---|---|
| MSB's | U15 | U17 |
| LSB's | U14 | U16 |

A 0 and a 1 can be written into every display memory location as follows:

a. Enter $^{c}$CLEAR to clear the screen.

b. Enter $^{c}$0. The screen should fill with background U's. The bit pattern is 01010101.

c. Hold the RETURN key down until at least two rows scroll up off the display.

d. Move the cursor up into the field of characters and enter two LINE/INS's. Two rows of characters should move down into the previously blank rows.

e. Enter $^{c}$0. The display should fill with foreground *'s. The bit pattern is 10101010.

f. Repeat steps c and d.

### 3.4.4 Keyboard

If a single key does not operate, the keyswitch is probably defective. Keyswitches may be replaced as described in paragraphg 3.3.7.

If a group of keys does not function, check for cold solder joints or bad connections. Also compare the non-operating keys with figure C-5. If the keys have a common X coordinate, the fault is probably in U23 or U20. If they have a common Y coordinate, the fault is probably in U22.

### 3.4.5 Monitor

Refer to figure 3-3 for monitor troubleshooting.

## 3.5 CIRCUIT DIFFERENCES

Some component values on the logic board may not agree with the schematic diagram, and some components may have been added to correct specific problems. If these components should fail, it is recommended that they be replaced with the same type and value. Some examples are given in table 3-4.

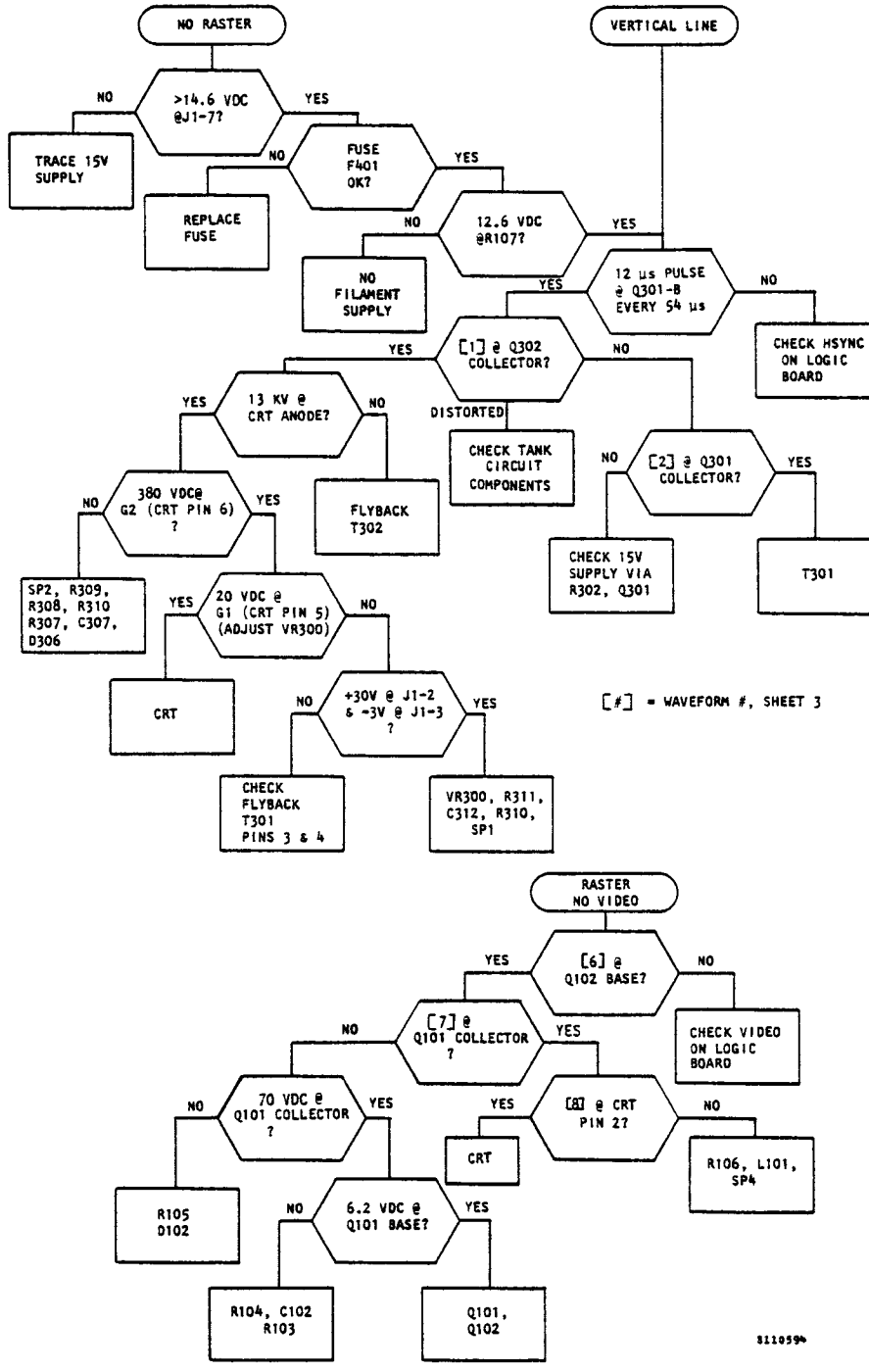



Figure 3-3. Monitor Troubleshooting Guide (Sheet 1 of 3)

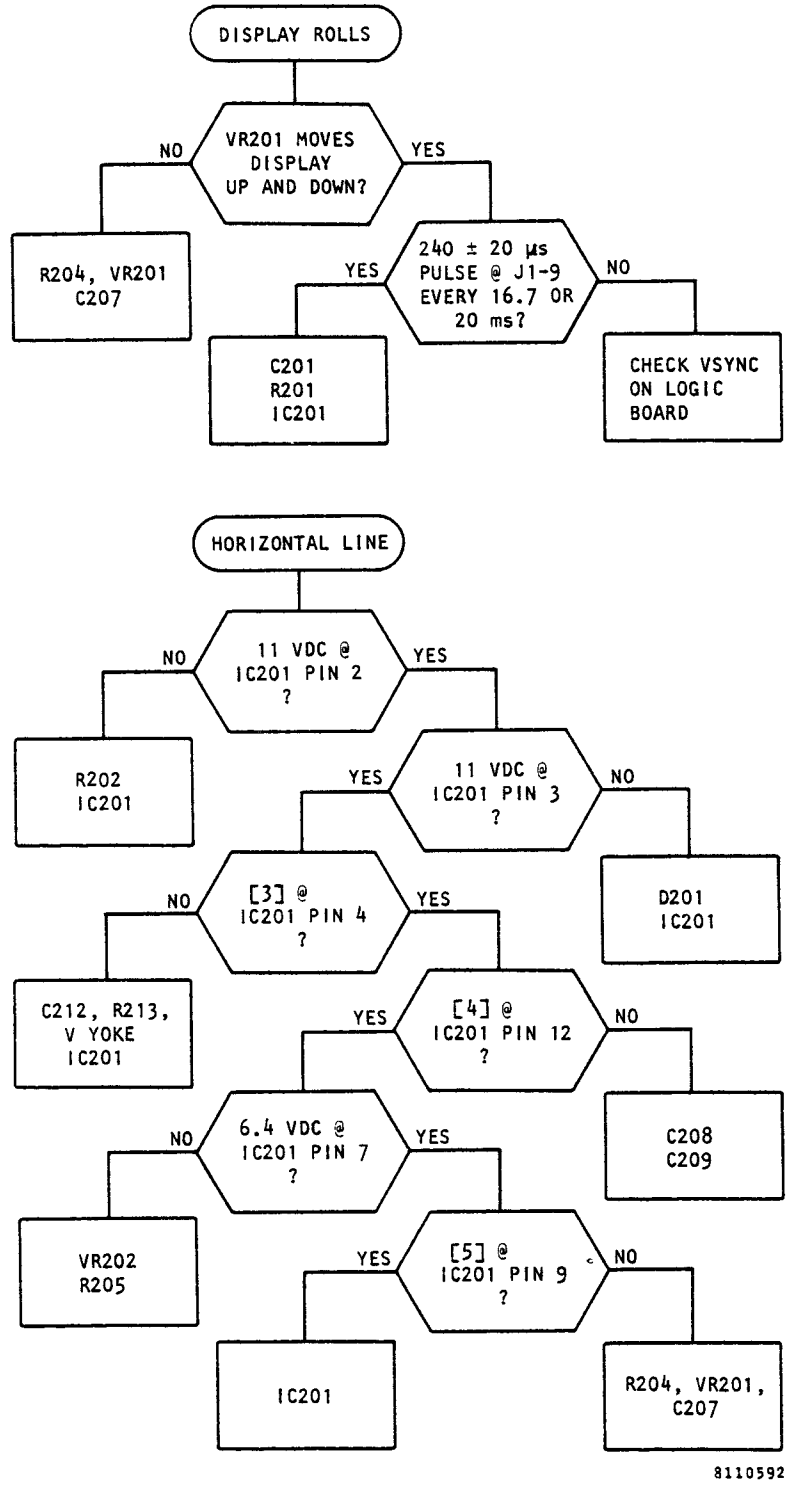
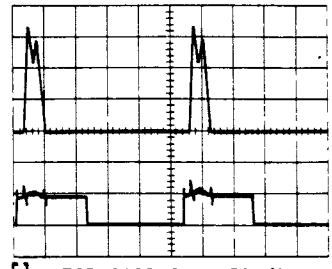
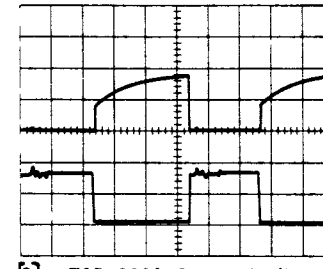


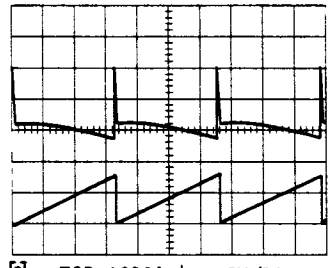

Figure 3-3. Monitor Troubleshooting Guide (Sheet 2 of 3)



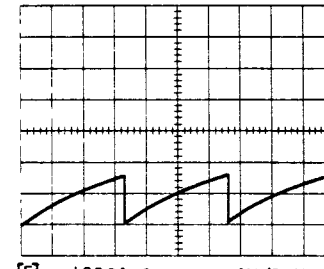
[1] TOP Q302-C 50V/DIV
BOT Q301-B 1 V/DIV
10µS/DIV



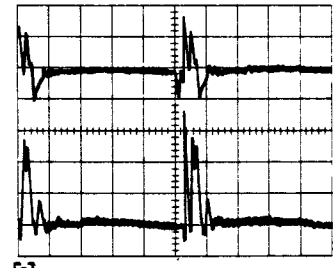
[2] TOP Q301-C 10V/DIV
BOT H DRIVE 2V/DIV
10 µS/DIV



[3] TOP IC201-4 5V/DIV
[4] BOT IC201-12 2V/DIV
5ms/DIV



[5] IC201-9 1V/DIV
5ms/DIV



[8] TOP CRT PIN 2 0.2V/DIV
[7] TOP Q101-C 0.2V/DIV
[6] BOT Q102-B 0.1V/DIV
10µS/DIV
BLOCK CURSOR ONLY DISPLAYED

NOTE: USE AC COUPLING FOR [7] AND [8]

8112206

Figure 3-3. Monitor Troubleshooting Guide (Sheet 3 of 3)

Table 3-4. Component Differences

| Location | Difference | Purpose |
|---|---|---|
| C3 | Value may be 0.0033 uF instead of 0.0022 uF | Adjust IRQ pulse width |
| U6 | 150 pF ceramic capacitor from pin 12 to pin 8 (ground) | Correct timing problem which causes data from top half of display to be written into bottom half, when insert and delete line are used. |
| U7 | 470 pF ceramic capacitor from pin 9 to pin 8 (ground) | Correct timing problem resulting in missing address strobe. |
| U31 | 1N4148 diode from pin 5 (cathode) to ground | Correct video jitter problem |
| J3 | 0.01 uF ceramic capacitor at pins 2 and 1 | Suppress noise on H Sync signal |
| C1 | Reduce value to 2.2 uF or 1 uF | Eliminate power-up reset failure |

# SECTION 4

## PARTS DATA

Type numbers for electronic components are provided on the schematic diagrams in Appendix C. This section provides part numbers for assemblies and Hazeltine part numbers for components which may not be available locally or in small quantities.

### CHASSIS COMPONENTS

| Part Number | Description |
|---|---|
| | **Piece Parts** |
| PC-01-009 | Top Cover Assy. |
| PC-01-010 | Bottom Cover Assy. |
| XF-01-024L | Power Transformer, 115V/60Hz |
| XF-01-024M | Power Transformer, 230V/50Hz |
| XF-01-024J | Power Transformer, 110V/50Hz |
| CR-03-012 | CRT |
| LN-07-006 | Coils, Yoke |
| FU-01-019 | Fuse, 1.5A |
| FU-03-003 | Fuse Holder |
| 1SPS912911 | Transistor, MJ2955 |
| SW-08-001 | Power Switch |
| KJ-06-026 | Cable, 16 Pin Flat, P4 |
| KJ-01-049 | Cable, Power Transistor, 3 Pin, P9, P10 |
| KJ-01-044B | Cable, Power Supply to Logic Bd, P6, P8 |
| KJ-01-043 | Cable, Speaker, P5 |
| KJ-01-044A | Cable, Transformer, P7 |
| KJ-01-040 | Cable, V Yoke |
| KJ-01-041 | Cable, H Yoke |
| KJ-01-064 | Cable, Logic Bd to Monitor, P3/P1 |
| | **Assemblies** |
| KP-801 | Keyboard |
| PP-801 | Power Supply Board |
| MP-801 | Monitor Board |
| LP-801 | Main Logic Board |

093 2-
46433
01-568-1851

27533

## LOGIC BOARD COMPONENTS

| Ref. Des. | Description | Part Number |
|---|---|---|
| D1, D2 | Diode | IN4148 |
| D4 | Zener Diode, 12V, ½W | SM-02-022 |
| DIP1 | DIP Switch, 10 part | SW-09-006 |
| DIP2 | DIP Switch, 8 part | SW-09-005 |
| J1, J2 | EIA Connector | KJ-06-025 |
| R38 | Resistor, Variable, 500 ohm | VR-02-040 |
| U4, U5 | IC, SN74LS93 | 1SPS912970 |
| U6 | IC, SN74LS175 | 1SPS912703 |
| U7, U29, U30 | IC, SN74LS174 | 1SPS912794 |
| U8 | IC, R6502 | SM-03-500 |
| U9 | IC, SN74LS245 | 1SPS912978 |
| U10 | IC, SN74LS139 | 1SPS912793 |
| U11, U12, U13 | IC, SN74LS157 | 1SPS912702 |
| U19 | Program ROM, 60 Hz | SM-03-580-1 |
| U19 | Program ROM, 50 Hz | SM-03-580-2 |
| U20 | IC, R6531-098P | SM-03-501 |
| U21, U22 | IC, SN74LS244 | 1SPS912843 |
| U24 | IC, MC6845P | 1SPS912848 |
| U25 | IC, SN74LS373 | 1SPS912855 |
| U26 | Char. Gen. ROM | SM-03-526 |
| U27 | IC, SN74LS123 | SM-03-512 |
| U28 | IC, SN74LS166 | 1SPS912975 |
| U31 | IC, SN74LS14 | SM-03-519 |
| U39 | IC, 4N25 | SM-03-528 |
| U40 | IC, MC6850P | SM-03-503 |
| U41, U43 | IC, 1489 | 1SPS910072 |
| U42, U44 | IC, 1488 | 1SPS910071 |
| U45 | IC, 4N33 | SM-03-529 |
| Y1 | Crystal, 16.5888 MHz | XT-01-008 |

## MONITOR BOARD COMPONENTS

| Ref. Des. | Description | Part Number |
|---|---|---|
| C303 | Capacitor, 22 F, 25V | CA-076-226 |
| D101 | Diode, 11-Z6V2 | SM-02-092 |
| D102, D304, D305 | Diode, RGP10D | SM-02-090 |
| D201 | Diode | IN4001 |
| D301, D302, D307 | Diode, RGP10G | SM-02-032 |
| D306 | Diode, RGP10K | SM-02-014 |
| IC201 | IC, TDA1170 | 1SPS912823 |
| L101 | Coil, Choke | LN-04-001 |
| L301 | Coil, Horiz Linearity | LN-06-002 |
| L302 | Coil, Width | LN-09-003 |
| L303 | Coil, Peaking | LN-14-017 |
| Q101 | Transistor, 2SC1921 | SM-01-021 |
| Q102 | Transistor, 2SC461B | SM-01-016 |
| Q301 | Transistor, 2SC1213A | SM-01-017 |
| Q302 | Transistor, 2SC681A | SM-01-039 |
| T301 | Transformer, Horiz Drive | XF-07-006 |
| T302 | Flyback Transformer | XF-02-008 |
| VR201, VR203, VR300 | Resistor, Variable, 100K | VR-04-032 |
| VR202 | Resistor, Variable, 250K | VR-04-033 |
| XVI | CRT Socket | KJ-06-028 |

## POWER SUPPLY COMPONENTS

| Ref. Des. | Description | Part Number |
|---|---|---|
| C50 | Capacitor, 10,000 uF, 25V | CA-004-109 |
| C51 | Capacitor, 10,000 uF, 35V | CA-005-109 |
| C52 | Capacitor, 4700 uF, 25V | CA-004-478 |
| D50, D51 | Bridge Rectifier, KBPC6005 | SM-02-077 |
| D52 | Bridge Rectifier, W005M | SM-02-076 |
| Q53, Q54 | Transistor, 2N4037 | SM-01-091 |
| U50 | Regulator, MC7805CT | SM-03-032 |
| U51 | Regulator, MC7912CT | 1SPS331804-12 |
| U52 | Regulator, MC7815CT | 1SPS331879 |

## KEYBOARD COMPONENTS

| Ref. Des. | Description | Part Number |
|---|---|---|
| D5, D7 | Light Emitting Diode | LP-01-001 |
| D8, D10 | Diode | IN4148 |
| U23 | IC, SN7445N | SM-03-515 |
| - | Keyswitch, CAPS Lock<br>SW-06-001A-S2[2] | SW-06-001-S2[1] |
| - | Keyswitch, Momentary<br>SW-06-001A-S1[2] | SW-06-001-S1[1] |
| - | Keycap Set<br>SW-06-001A-C[2] | SW-06-001-C[1] |

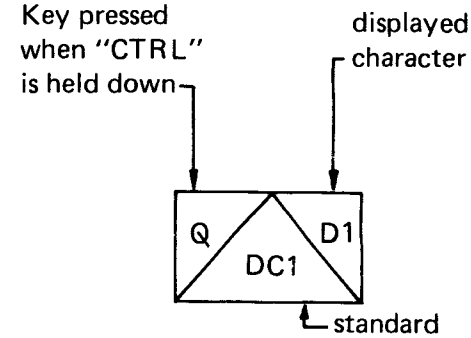
1. For unit serial Nos. 2,000,700 and below
2. For unit serial Nos. 2,000,701 and up

# APPENDIX A

## ASCII CODE

| ROW | COL / BIT | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|---|
| | BIT (7 6 5) | 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 |
| 0 | (4 3 2 1) 0000 | @ / $N_U$ NUL | P / $D_L$ DLE | SP | 0 | @ | P | ` | P |
| 1 | 0001 | A / $S_H$ SOH | Q / $D_1$ DC1 | ! | 1 | A | Q | a | q |
| 2 | 0010 | B / $S_X$ STX | R / $D_2$ DC2 | " | 2 | B | R | b | r |
| 3 | 0011 | C / $E_X$ ETX | S / $D_3$ DC3 | # | 3 | C | S | c | s |
| 4 | 0100 | D / $E_T$ EOT | T / $D_4$ DC4 | $ | 4 | D | T | d | t |
| 5 | 0101 | E / $E_Q$ ENQ | U / $N_K$ NAK | % | 5 | E | U | e | u |
| 6 | 0110 | F / $A_K$ ACK | V / $S_Y$ SYN | & | 6 | F | V | f | v |
| 7 | 0111 | G / $B_L$ BEL | W / $E_B$ ETB | ' | 7 | G | W | g | w |
| 8 | 1000 | H / $B_S$ BS | X / $C_N$ CAN | ( | 8 | H | X | h | x |
| 9 | 1001 | I / $H_T$ HT | Y / $E_M$ EM | ) | 9 | I | Y | i | y |
| A | 1010 | J / $L_F$ LF | Z / $S_B$ SUB | * | : | J | Z | j | z |
| B | 1011 | K / $V_T$ VT | [ / $E_C$ ESC | + | ; | K | [ | k | { |
| C | 1100 | L / $F_F$ FF | \ / $F_S$ FS | , | < | L | \ | l | ¦ |
| D | 1101 | M / $C_R$ CR | ] / $G_S$ GS | – | = | M | ] | m | } |
| E | 1110 | N / $S_O$ SO | ^ / $R_S$ RS | . | > | N | ^ | n | ~ |
| F | 1111 | O / $S_I$ SI | – / $U_S$ US | / | ? | O | _ | o | DEL |

$A_K$ –ACKNOWLEDGE
$B_L$ –BELL
$B_S$ –BACKSPACE
$C_N$ –CANCEL LINE
$C_R$ –CARRIAGE RETURN
$D_L$ –DATA LINK ESCAPE
$D_1$ –DEVICE CONTROL 1
$D_2$ –DEVICE CONTROL 2
$D_3$ –DEVICE CONTROL 3
$D_4$ –DEVICE CONTROL 4
$E_M$ –END OF MEDIUM
$E_Q$ –ENQUIRY
$E_X$ –END OF TRANSMISSION
$E_S$ –ESCAPE
$E_B$ –END OF BLOCK
$E_T$ –END OF TEXT
$F_F$ –FORM FEED
$F_S$ –FILE SEPARATOR
$G_S$ –GROUP SEPARATOR
$H_T$ –HORIZONTAL TAB
$L_F$ –LINE FEED
$N_K$ –NEGATIVE ACKNOWLEDGE
$R_S$ –RECORD SEPARATOR
$S_1$ –SHIFT IN
$S_O$ –SHIFT OUT
$S_P$ –SPACE
$S_H$ –START OF HEADING
$S_T$ –START OF TEXT
$S_B$ –SUBSTITUTE
$S_Y$ –SYNCHRONOUS IDLE
$U_S$ –UNIT SEPARATOR
$V_T$ –VERTICAL TAB




CONTROL CHARACTER LEGEND

# APPENDIX B
# SUMMARY OF REMOTE COMMANDS

| Command | Hazeltine | | | Regent 25 | | | ADM-3A | | |
|---|---|---|---|---|---|---|---|---|---|
| | Lead In? | ASCII | Key-stroke | Lead In? | ASCII | Key-stroke | Lead In? | ASCII | Key-stroke |
| Direct Cursor Address | Yes | DC1 | ^Q | Yes | Y | Y | -- | -- | -- |
| Send Cursor Address | Yes | ENQ | ^E | -- | -- | -- | -- | -- | -- |
| Horizontal Address | -- | -- | -- | No | DLE | ^P | -- | -- | -- |
| Vertical Address | -- | -- | -- | No | VT | ^K | -- | -- | -- |
| Cursor Up | Yes | FF | ^L | No | SUB | ^Z | No | VT | ^K |
| Cursor Down | Yes | VT | ^K | -- | -- | -- | -- | -- | -- |
| Cursor Right | No | DLE | ^P | No | ACK | ^F | No | FF | ^L |
| Cursor Left | No | BS | ^H | No | NAK | ^U | No | BS | ^H |
| Cursor Home | Yes | DC2 | ^R | No | SOH | ^A | No | RS | ^^ |
| Carriage Return | No | CR | ^M | No | CR | ^M | No | CR | ^M |
| Line Feed | No | LF | ^J | No | LF | ^J | No | LF | ^J |
| Field Tab | No | HT | ^I | -- | -- | -- | -- | -- | -- |
| Reverse Field Tab | Yes | DC4 | ^T | -- | -- | -- | -- | -- | -- |
| Horizontal Tab | Yes | : | Colon | -- | -- | -- | -- | -- | -- |
| Enter Block Mode | Yes | # | # | -- | -- | -- | -- | -- | -- |
| Enter Line Mode | Yes | . | Period | -- | -- | -- | -- | -- | -- |
| Enter Normal Mode | Yes | $ | $ | -- | -- | -- | -- | -- | -- |
| Function Keypad Mode 1 | Yes | ; | Semi-colon | Yes | ; | Semi-colon | Yes | ; | Semi-colon |
| Function Keypad Mode 2 | Yes | < | < | Yes | < | < | Yes | < | < |
| Function Keypad Mode 3 | Yes | = | = | Yes | = | = | -- | -- | -- |
| Exit Function Keypad Mode | Yes | > | > | Yes | > | > | Yes | > | > |
| Foreground Follows | Yes | US | ^(under-line) | -- | -- | -- | -- | -- | -- |
| Background Follows | Yes | EM | ^Y | -- | -- | -- | -- | -- | -- |
| Clear Field | Yes | SYN | ^V | -- | -- | -- | -- | -- | -- |

| Command | Hazeltine | | | Regent 25 | | | ADM-3A | | |
|---|---|---|---|---|---|---|---|---|---|
| | Lead In? | ASCII | Key-stroke | Lead In? | ASCII | Key-stroke | Lead In? | ASCII | Key-stroke |
| Clear to End of Line | Yes | SI | ^O | Yes | K | K | -- | -- | -- |
| Clear to End of Screen (Foreground) | Yes | CAN | ^X | -- | -- | -- | -- | -- | -- |
| Clear to End of Screen (Background) | Yes | ETB | ^W | Yes | k | k | -- | -- | -- |
| Clear Foreground | Yes | GS | ^ ] | -- | -- | -- | -- | -- | -- |
| Clear Screen | Yes | FS | ^ \ | No | FF | ^L | No | SUB | ^Z |
| Insert Line | Yes | SUB | ^Z | -- | -- | -- | -- | -- | -- |
| Delete Line | Yes | DC3 | ^S | -- | -- | -- | -- | -- | -- |
| Page Transmit | Yes | SO | ^N | -- | -- | -- | -- | -- | -- |
| Field Transmit | Yes | ) | ) | -- | -- | -- | -- | -- | -- |
| Transmit Character at Cursor | Yes | ! | ! | -- | -- | -- | -- | -- | -- |
| Enable Aux Out With Display | Yes | / | / | No | DC2 | ^R | -- | -- | -- |
| Enable Aux Out/ No Display | Yes | * | * | Yes | 3 | 3 | -- | -- | -- |
| Disable Aux Out | Yes | ? | ? | No | DC4 | ^T | -- | -- | -- |
| Transparent Print Off | -- | -- | -- | Yes | 4 | 4 | -- | -- | -- |
| Keyboard Lock | Yes | NAK | ^U | Yes | 5 | 5 | No | SI | ^O |
| Keyboard Unlock | Yes | ACK | ^F | Yes | 6 | 6 | No | SO | ^N |
| Sound Alarm | No | BEL | ^G | No | BEL | ^G | No | BEL | ^G |
| Display Test Pattern (H) | Yes | " | " | -- | -- | -- | -- | -- | -- |
| Display Character Font | Yes | 8 | 8 | -- | -- | -- | -- | -- | -- |

Lead In may be ESC or ~ for Hazeltine, must be ESC for Regent 25 or ADM-3A.

# APPENDIX C

## DIAGRAMS

This section contains interconnection and schematic diagrams for the terminal and its subassemblies.

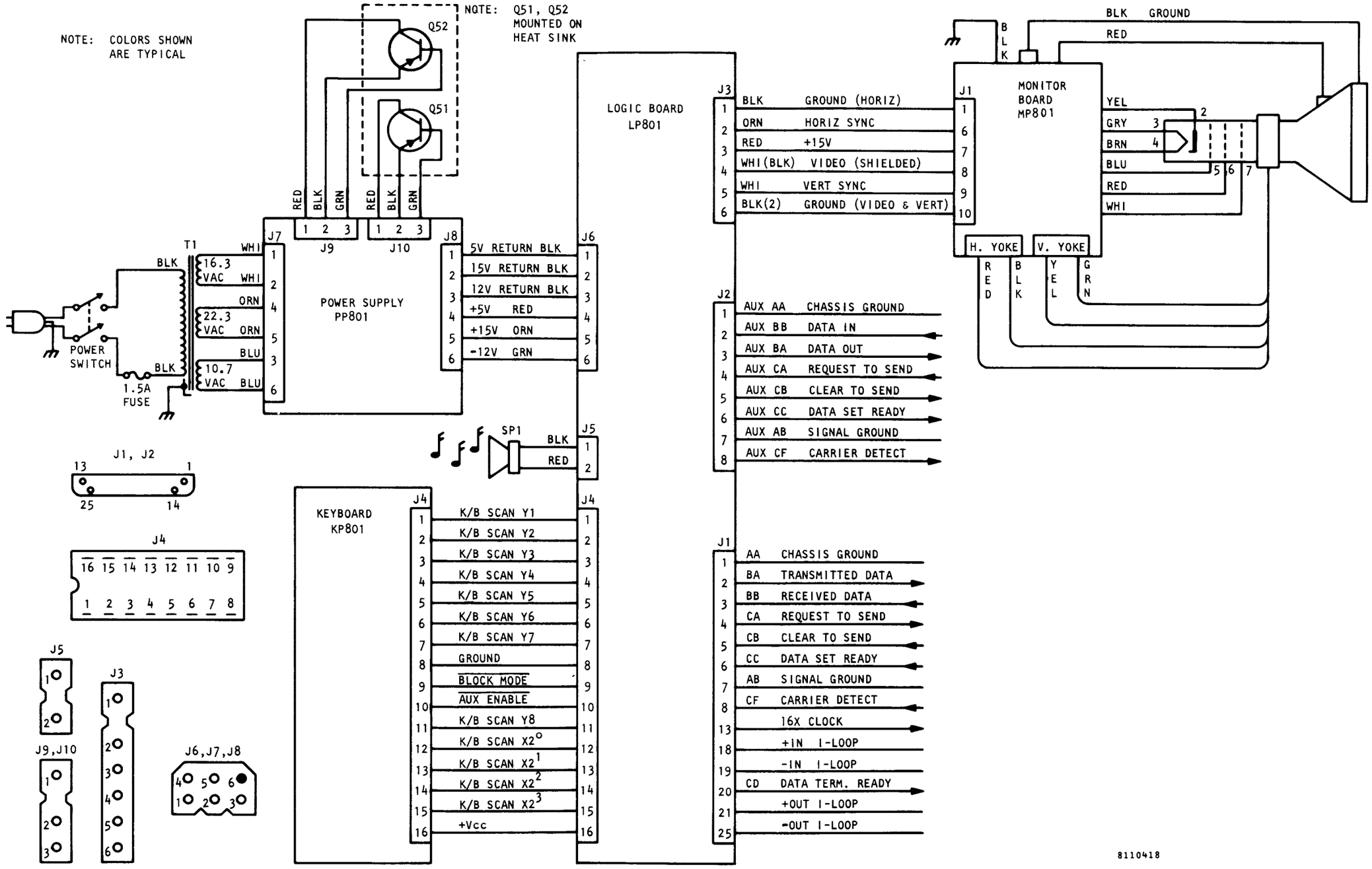



Figure C-1. **Interconnection Diagram**

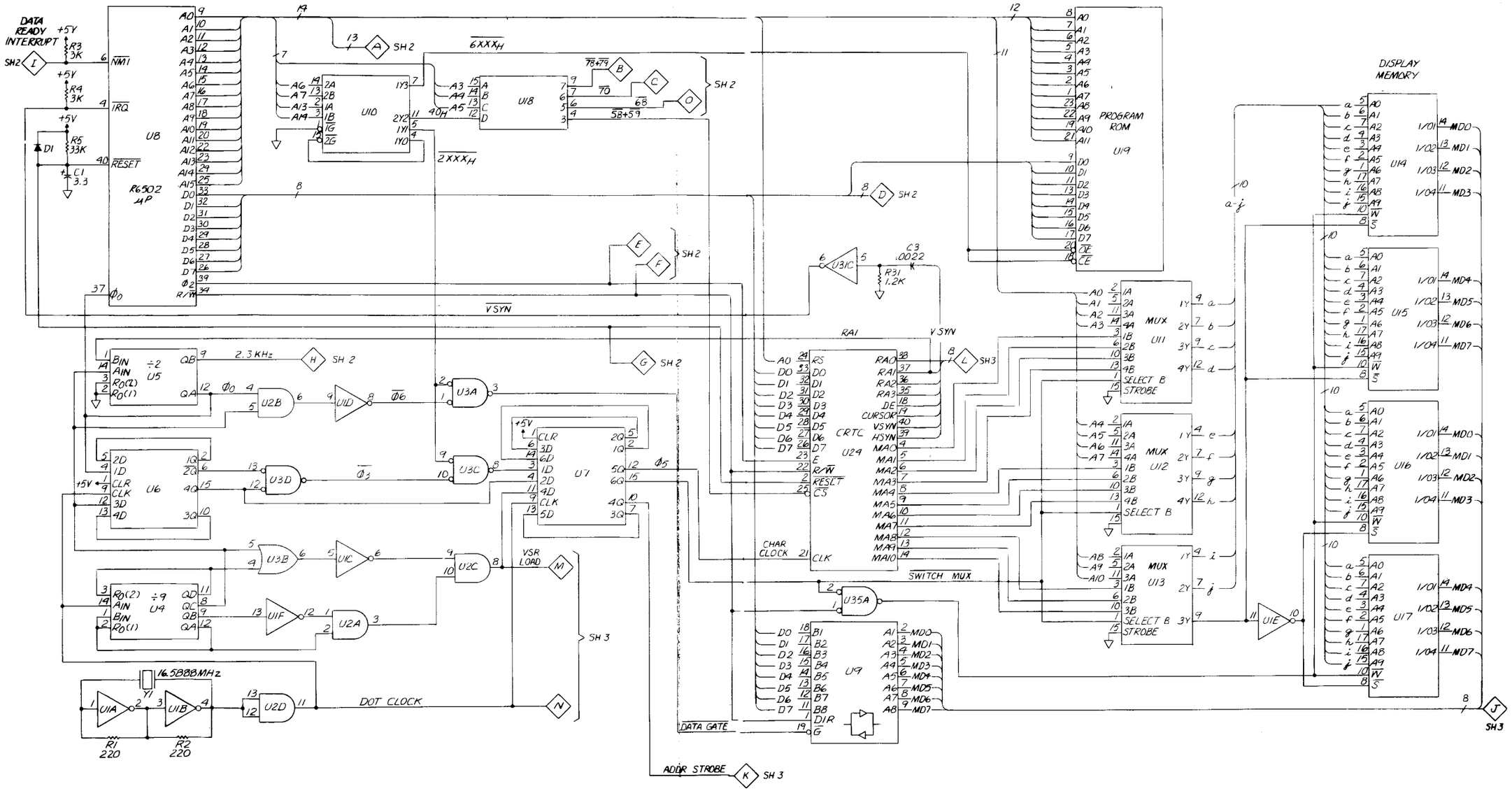



Figure C-2. **Logic Board Schematic Diagram** (Sheet 1 of 3)

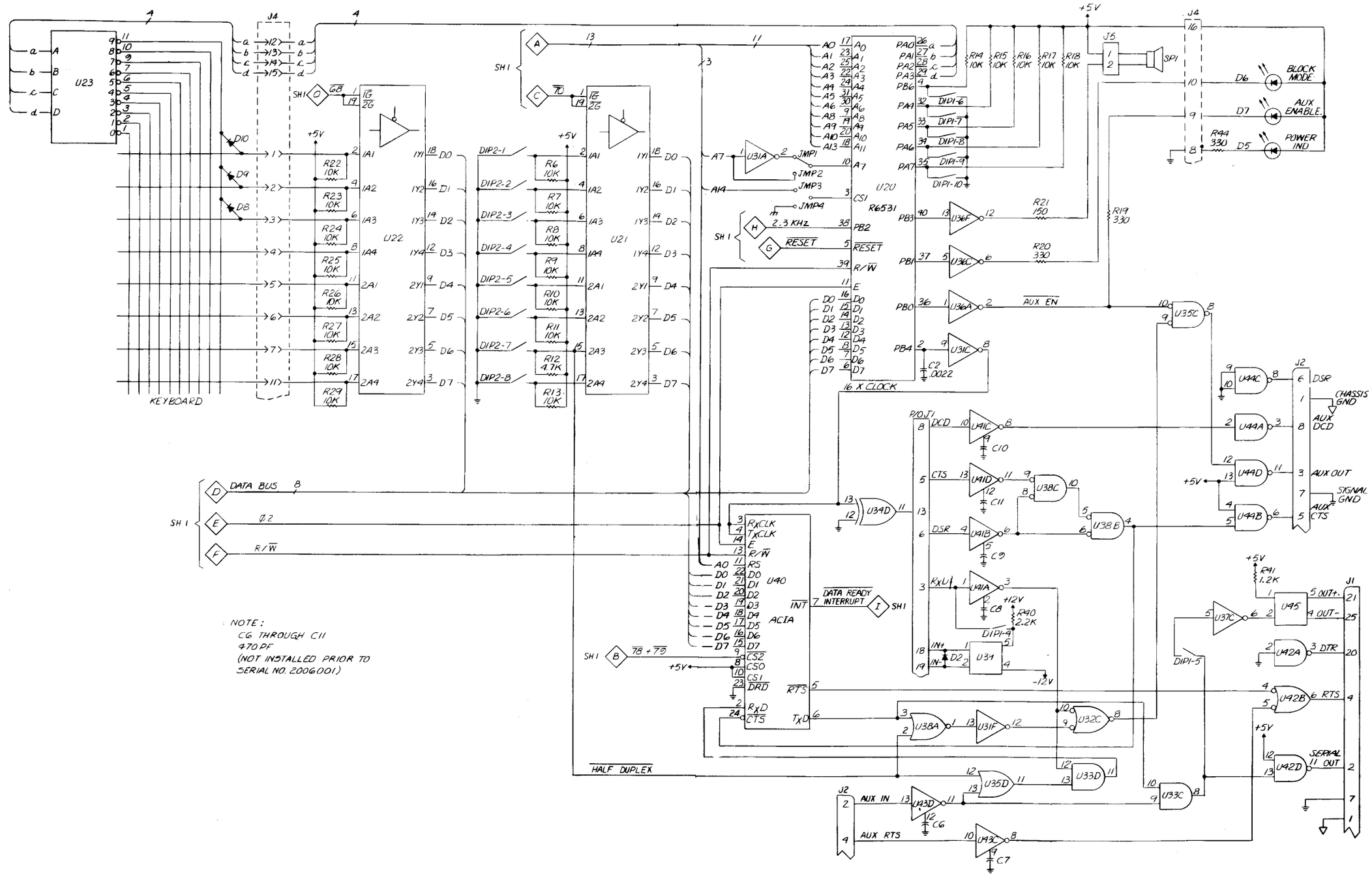
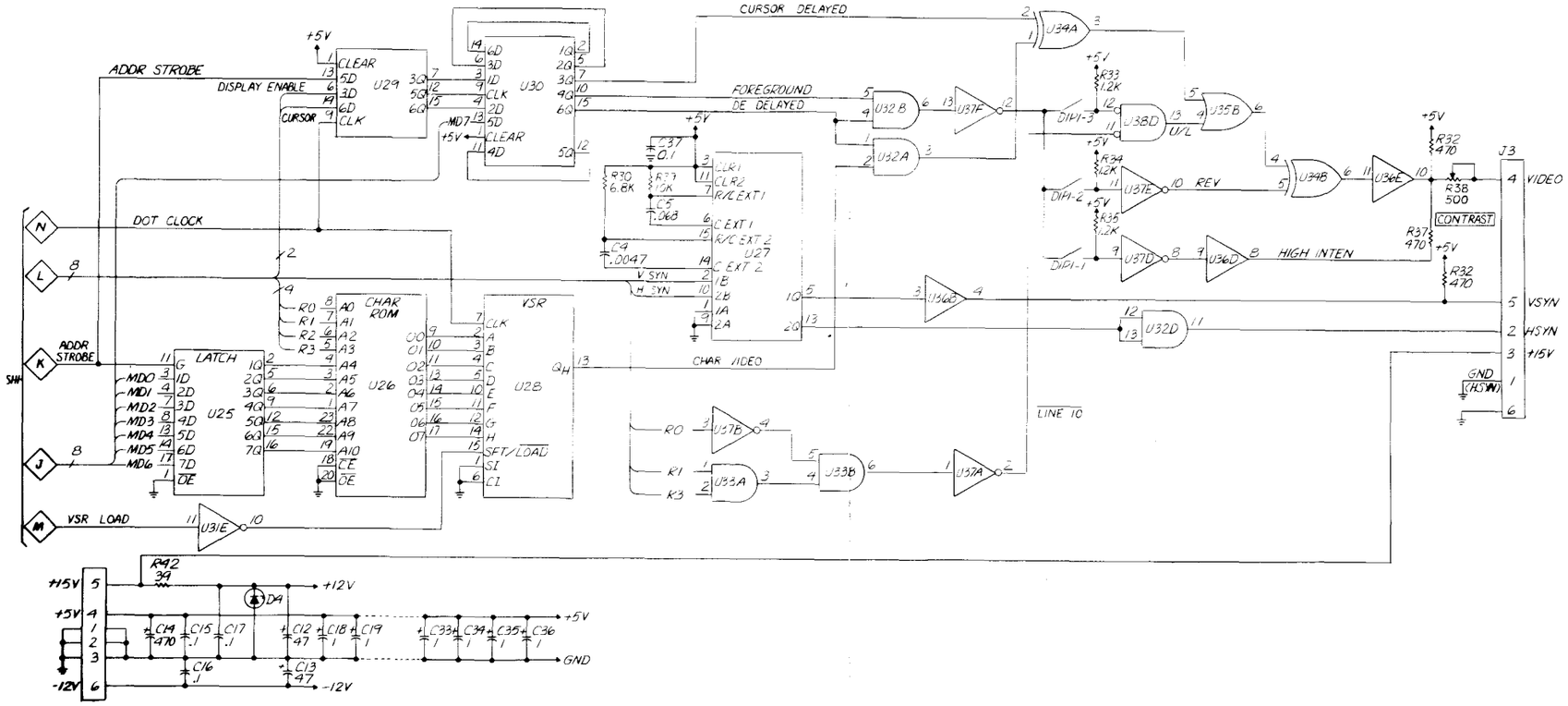



Figure C-2. **Logic Board Schematic Diagram (Sheet 2 of 3)**




NOTES:
1. UNLESS OTHERWISE STATED:
   ALL RESISTANCES ARE IN OHMS, 1/4 W, 5%
   ALL CAPACITANCES ARE IN MICROFARADS
2. INTEGRATED CIRCUIT TYPES AND THEIR CONNECTIONS FOR POWER AND GROUND ARE AS FOLLOWS:

| REFERENCE DESIGNATION | PART NO. | -12 | +12 | +5 | GND |
|---|---|---|---|---|---|
| U1, U37 | 74LS04 | | | 14 | 7 |
| U2, U32, U33 | 74LS08N | | | 14 | 7 |
| U3, U35 | 74LS32 | | | 14 | 7 |
| U4, U5 | 74LS93 | | | 5 | 10 |
| U6 | 74LS175 | | | 16 | 8 |
| U7, U27, U30 | 74LS174 | | | 16 | 8 |
| U8 | R6502 | | | 1,21 | 8 |
| U9 | 74LS245 | | | 20 | 10 |
| U10 | 74LS139 | | | 16 | 8 |
| U11, U12, U13 | 74LS157 | | | 16 | 8 |
| U14, U15, U16, U17 | MCM2114P20 | | | 18 | 9 |
| U18 | 74LS42 | | | 16 | 8 |
| U19 | 2732 | | | 24 | 12 |
| U20 | R6531-048P | | | 21 | 1 |
| U21, U22 | 74LS244 | | | 20 | 10 |
| U23 | 7495 | | | 16 | 8 |
| U24 | MC6845P | | | 20 | 1 |
| U25 | 74LS373 | | | 20 | 10 |
| U26 | 2716 | | | 24 | 12 |
| U27 | 74LS123 | | | 16 | 8 |
| U28 | 74LS166 | | | 16 | 8 |
| U31 | 74LS14 | | | 14 | 7 |
| U34 | 74LS86 | | | 14 | 7 |
| U36 | 7417 | | | 14 | 7 |
| U38 | 74LS02 | | | 14 | 7 |
| U39 | 4N25 | | | N/A | N/A |
| U40 | MC6850P | | | 1 | 12 |
| U41, U43 | 1489 | | | 14 | 7 |
| U42, U44 | 1488 | 7 | 14 | N/A | N/A |
| U45 | 4N33 | N/A | N/A | N/A | N/A |

Figure C-2. **Logic Board Schematic Diagram** (Sheet 3 of 3)